Unit – I

Objectives:

- To familiarize with the operation, characteristics, types and applications of various p-n junctions and metal-semiconductor junctions.

Syllabus:

Diffusion and recombination - the continuity equation, equilibrium conditions, forward and reverse-biased junctions, reverse-bias breakdown, The ideal diode, terminal characteristics of junction diodes, Metal-semiconductor junctions, ideal MOS capacitor, MOS capacitance-voltage analysis, Special diodes.

Outcomes:

At the end of the unit, student will be able to

- analyze the carrier transport in junctions
- understand the formation, operation and characteristics of different types of junctions.
- analyze the behavior of MOS capacitor.
- distinguish the properties of semiconductor junctions and metal-semiconductor junctions. .

Learning Material

1.1 Diffusion and Recombination - the Continuity Equation

- Electrons and holes cannot mysteriously appear or disappear at a given point, but must be transported to or created at the given point via some type of carrier action.
- **Diffusion:** When excess carriers are created non uniformly in a semiconductor, the electron and hole concentrations vary with position in the sample. Any spatial variation (gradient) in n and p calls for a net motion of the carriers from regions of high carrier concentration to regions of low carrier concentration..This type of motion is called is called Diffusion.
- Two basic processes of current conduction are diffusion and drift. Diffusion due to a carrier gradient and drift due to an electric field.
- **Recombination:** Recombination is a process that occurs in semiconductor when an electron in the conduction band makes a transition (direct or indirect) to an empty state (hole) in the valance band. But recombination process is a temperature dependent.
- The description of conduction process in semiconductors includes the recombination effect because recombination can cause a variation in the carrier distribution.
- **Continuity Equation**: The continuity equation describes a basic concept, namely that a change in carrier density over time is due to the difference between the incoming and outgoing flux of carriers plus the generation and minus the recombination.
- Consider a 1D case, a semiconductor sample differential length - Δx with area A in the yz plane shown in Fig 1.1
- The hole current density leaving the volume $J_p(x+\Delta x)$, can be larger or smaller than the current density entering $J_p(x)$, depending on the generation and recombination of carriers taking place within the volume.
- The net increase in hole concentration per unit time, $\frac{\partial p}{\partial t}$, is the difference between the hole flux per unit volume entering and leaving, minus the recombination rate.
- We can convert hole current density to hole particle flux density by dividing $J_{p,}$ by q.

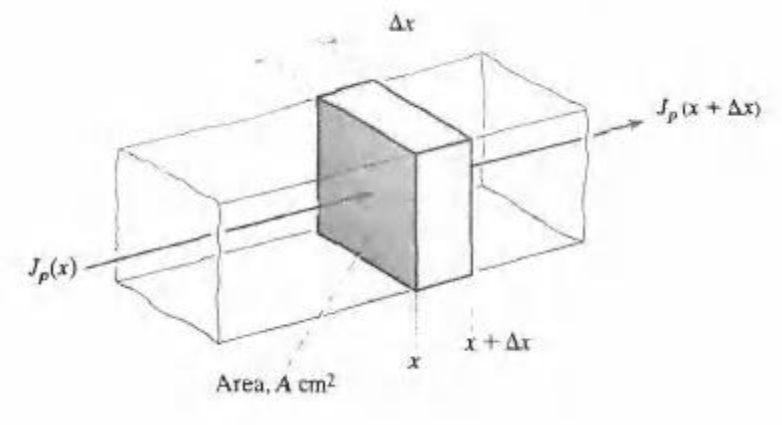


Fig 1.1 Current entering and leaving a volume ΔxA

- The current densities are already expressed per unit area. Thus dividing $Jp(x)/q$ by Δx gives the number of carriers per unit volume entering ΔxA per unit time, and (1/q)Jp(x+ Δx)/Δx is the number leaving per unit volume and time:

$$\left.\frac{\partial p}{\partial t}\right|_{x\to x+\Delta x} = \frac{1}{q}\frac{J_p(x) - J_p(x+\Delta x)}{\Delta x} - \frac{\delta p}{\tau_p} \qquad \text{-------- (1.1)}$$

Rate of hole buildup = increase of hole concentration in $\delta x A$ per unit time − recombination rate

- As Δx approaches to zero, we can write current change in derivative form :

$$\frac{\partial p(x,t)}{\partial t} = \frac{\partial \delta p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} - \frac{\delta p}{\tau_p} \qquad \text{--------- (1.2)}$$

- The expression 1.2 is called the continuity equation for holes.
- The continuity equation for electrons we can write (same as equation 1.2 except sign due to negative charge of electron)

$$\frac{\partial \delta n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} - \frac{\delta n}{\tau_n} \qquad \text{---------- (1.3)}$$

- When current is carried strictly by diffusion (neglect drift), we can replace the currents in Eqs.(1-2) by the expression for diffusion current. electron diffusion current. we have,

$$J_n(\text{diff.}) = qD_n\frac{\partial \delta n}{\partial x} \qquad \text{---------- (1.4)}$$

- Substitute Eqs 1-4 in Eqs 1-3 we obtain the diffusion equation for electrons ,

$$\frac{\partial \delta n}{\partial t} = D_n \frac{\partial^2 \delta n}{\partial x^2} - \frac{\delta n}{\tau_n}$$

- And similarly for holes,

$$\frac{\partial \delta p}{\partial t} = D_p \frac{\partial^2 \delta p}{\partial x^2} - \frac{\delta p}{\tau_n}$$

- These equations are useful in solving transient problems of diffusion with recombination

1.2 Equilibrium Conditions

1.2.1 The Contact Potential

- Let us consider separate regions of p- and n-type semiconductor material, and brought together to form a junction. Before they are joined, the n material has a large concentration of electrons and few holes, whereas, in the p material holes are in large density and electrons are few.
- Upon joining the two regions, diffusion of carriers take place because of the large carrier concentration gradients at the junction. Thus holes diffuse from the p side into the n side, and electrons diffuse from n to p. The resulting diffusion current cannot build up indefinitely, however, because an opposing electric field is created at the junction as shown in Fig. 1.2.
- The electrons diffusing from n to p leave behind uncompensated donor ions (N_d^+) in the n material and holes leaving the p region leave behind uncompensated acceptor ions (N_a^-).
- Hence a region of positive space charge is developed near the n side of the junction and negative charge near the p side as shown in Fig.1.2.
- The resulting electric field is directed from the positive charge toward the negative charge. Thus the electric field, $\mathscr{E}$ is in the direction opposite to that of diffusion current for each type of carrier (recall electron current is opposite to the direction of electron flow).
- Therefore the field creates a drift component of current from n to p, opposing the diffusion current. Since there is no net current flow across the junction at equilibrium,

the current due to the drift of carriers in the electric field must exactly cancel the diffusion current.

- The drift and diffusion components of electrons and holes are:

$$J_p(\text{drift}) + J_p(\text{diff.}) = 0 \quad \text{---------- (1.5)}$$

$$J_n(\text{drift}) + J_n(\text{diff.}) = 0 \quad \text{---------- (1.6)}$$

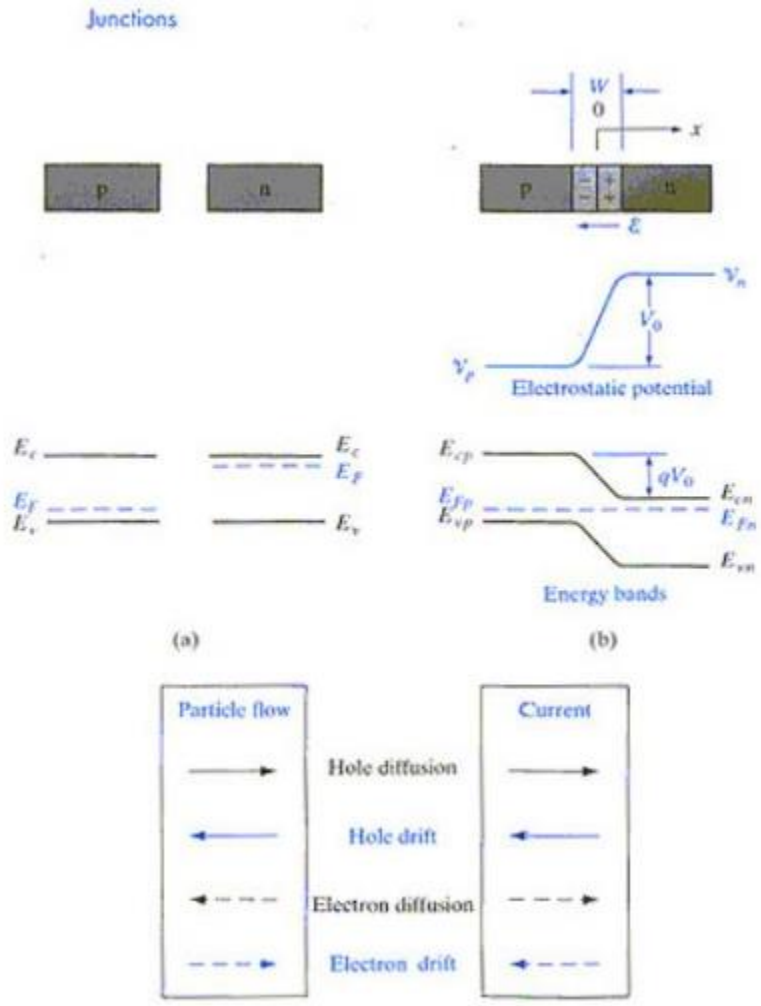


Fig. 1.2: Properties of an equilibrium p-n junction: (a) isolated, neutral regions of p-type and n-type material and energy bands for the isolated regions; (b) junction, showing space charge in the transition region W, the resulting electric field $\mathscr{E}$, contact potential V_0, and the separation of the energy bands; (c) directions of the four components of particle flow within the transition region and the resulting current directions.

- Thus, the electric field, $\mathscr{E}$ builds up to the point where the net current is zero at equilibrium. The electric field appears in space charge region W near the junction, and there is an equilibrium potential difference V_0 across W.
- In the electrostatic potential diagram of Fig. 1.2 b, there is a gradient in potential in the direction opposite to $\mathscr{E}$ in accordance with the fundamental relation:

$$\mathscr{E}(x) = -d\mathscr{V}(x)/dx$$

- If the electric field is zero in the neutral regions outside W, there is a constant potential V_n in the neutral n material, a constant potential V_p in the neutral p material, and a potential difference $V_0 = V_n - V_p$ between the two. The region W is called the **transition region** and the potential difference V_0 is called the **contact potential** or **built-in potential**.
- The contact potential separates the bands as shown in Fig. 1.2 b; the valence and conduction energy bands are higher on the p side of the junction than on the n side by the amount qV_0. The separation of the bands at equilibrium is required to make the Fermi level constant throughout the device.
- To obtain a quantitative relationship between V_0 and the doping concentrations on each side of the junction, equilibrium condition should be maintained in the drift and diffusion current components. The drift and diffusion components of the hole current just cancel at equilibrium:

$$J_p(x) = q\left[\mu_p p(x)\mathscr{E}(x) - D_p\frac{dp(x)}{dx}\right] = 0 \quad \text{--------} \quad (1.7)$$

$$\frac{\mu_p}{D_p}\mathscr{E}(x) = \frac{1}{p(x)}\frac{dp(x)}{dx} \quad \text{----------} \quad (1.8)$$

Where, the x-direction is arbitrarily taken from p to n. The electric field can be written in terms of the gradient in the potential,

$$\mathscr{E}(x) = -d\mathscr{V}(x)/dx$$

so that, Eq. (1.8) becomes

$$-\frac{q}{kT}\frac{dV(x)}{dx} = \frac{1}{p(x)}\frac{dp(x)}{dx} \quad \text{----------} \quad (1.9)$$

With the use of the Einstein relation for μ_p/D_p and integration of Eq. (1.9) gives

$$-\frac{q}{kT}\int_{V_p}^{V_n} dV = \int_{p_p}^{p_n}\frac{1}{p}dp$$

$$-\frac{q}{kT}(V_n - V_p) = \ln p_n - \ln p_p = \ln\frac{p_n}{p_p} \quad \text{---------- (1.10)}$$

- As the potential difference (V_n–V_p) is the contact potential V_0, in terms of the equilibrium hole concentrations on either side of the junction V_0 can be written as:

$$V_0 = \frac{kT}{q}\ln\frac{p_p}{p_n} \quad \text{---------- (1.11)}$$

- If we consider the step junction to be made up of material with N_a acceptors/cm^3 on the p side and a concentration of N_d donors/cm^3 on the n side, we can write Eq. (1.11) as

$$V_0 = \frac{kT}{q}\ln\frac{N_a}{n_i^2/N_d} = \frac{kT}{q}\ln\frac{N_aN_d}{n_i^2} \quad \text{---------- (1.12)}$$

by considering the majority carrier concentration as the doping concentration on each side, Eq. (1.11) can be modified as:

$$\frac{p_p}{p_n} = e^{qV_0/kT} \quad \text{---------- (1.13)}$$

- By using the equilibrium condition $p_p.n_p = n_i^2 = p_n.n_n$,the electron concentrations on either side of the junction are:

$$\boxed{\frac{p_p}{p_n} = \frac{n_n}{n_p} = e^{qV_0/kT}} \quad \text{---------- (1.14)}$$

1.2.2 Equilibrium Fermi Levels

- The Fermi level must be constant throughout the device at equilibrium (E_{Fn} — E_{Fp}= 0) and in terms of Fermi energy levels, the concentration of p_n and p_p are given by their equilibrium values

$$p_0 = N_v e^{-(E_F - E_v)/kT} \qquad \text{---------- (1.15)}$$

$$\frac{p_p}{p_n} = e^{qV_0/kT} = \frac{N_v e^{-(E_{Fp} - E_{vp})/kT}}{N_v e^{-(E_{Fn} - E_{vn})/kT}} \qquad \text{---------- (1.16)}$$

$$\Rightarrow e^{qV_0/kT} = e^{(E_{Fn} - E_{Fp})/kT} e^{(E_{vp} - E_{vn})/kT}$$

$$qV_0 = E_{vp} - E_{vn} \qquad \text{---------- (1.17)}$$

- From Fig. 1.2b the energy bands on either side of the junction are separated by the contact potential V_0 times the electronic charge q; thus the energy difference E_{vp} - E_{vn} is just equal to qV_0.
- When bias is applied to the junction, the potential barrier is raised or lowered from the value of the contact potential, and the Fermi levels on either side of the junction are shifted with respect to each other by an amount of applied voltage.

1.2.3 Space Charge at a Junction

- Within the transition region, electrons and holes are in transit from one side of the junction to the other. Some electrons diffuse from n to p, and some are swept by the electric field from p to n (and conversely for holes).
- There are however, very few carriers within the transition region at any given time and the space charge is developed within the transition region due to the uncompensated donor and acceptor ions.
- The charge density on the n side is just q times the concentration of donor ions N_d, and the negative charge density on the p side is -q times the concentration of acceptors N_a. The charge density within W is plotted in Fig. 1.3b.
- The transition region may extend into the p and n regions unequally, depending on the relative doping on the two sides. If the p side is more lightly doped than the n side (N_a<N_d), the space charge region must extend farther into the p material than into the n, to "uncover" an equivalent amount of charge.
- For a sample of cross-sectional area A, the total uncompensated charge on either side of the junction is

$$qAx_{p0}N_a = qAx_{n0}N_d \qquad \text{---------- (1.18)}$$

Where, xp_0 is the penetration of the space charge region into the p material, and xn_0 is the penetration into n. The total width of the transition region (W) is the sum of *xp0* and *xn0*.

- The electric field distribution within the transition region is calculated by using *Poisson's equation*, which relates the gradient of the electric field to the local space charge at any point x:

$$\frac{d\mathscr{E}(x)}{dx} = \frac{q}{\epsilon}(p - n + N_d^+ - N_a^-) \qquad \text{---------- (1.19)}$$

$$\frac{d\mathscr{E}}{dx} = \frac{q}{\epsilon}N_d, \qquad 0 < x < x_{n0} \qquad \text{---------- (1.20)}$$

$$\frac{d\mathscr{E}}{dx} = -\frac{q}{\epsilon}N_a, \qquad -x_{p0} < x < 0 \qquad \text{----------(1.21)}$$

Since, the contribution of the carriers (p - n) are neglected.

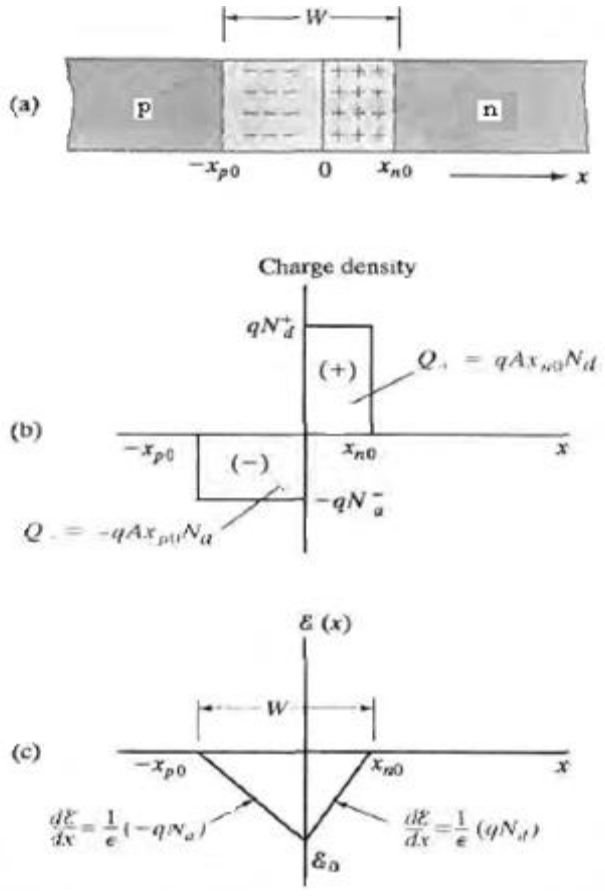


Fig. 1.3: Space charge and electric field distribution within the transition region of a p-n junction with $N_d > N_a$: (a) the transition region, with x = 0 defined at the metallurgical

junction; (b) charge density within the transition region, neglecting the free carriers; (c) the electric field distribution, where the reference direction for $\mathscr{E}$ is arbitrarily taken as the +x-direction.

- We can see from these two equations Eq. (1.20 &1.21) that a plot of $\mathscr{E}(x)$ vs. x within the transition region has two slopes, positive ($\mathscr{E}$ increasing with x) on the n side and negative on the p side. There is some maximum value of the field $\mathscr{E}_0$ at x= 0 (the metallurgical junction between the p and n materials), and $\mathscr{E}(x)$ is everywhere negative within the transition region as shown in Fig. 1.3 c.
- The electric field $\mathscr{E}(x)$ to be negative throughout W, since the electric field actually points in the $-x$ direction, from n to p. The electric field is assumed to go to zero at the edges of the transition region andit must be a maximum value ($\mathscr{E}_0$) at the junction, since this point is betweenthe charges Q+ and Q-on either side of the transition region.
- The value of $\mathscr{E}_0$ can be found by integrating either part of Eq. (1.20) with appropriate limits (see Fig. 1.3c in choosing the limits of integration).

$$\int_{\mathscr{E}_0}^{0} d\mathscr{E} = \frac{q}{\epsilon} N_d \int_{0}^{x_{n0}} dx, \qquad 0 < x < x_{n0} \qquad \text{---------- (1.22a)}$$

$$\int_{0}^{\mathscr{E}_0} d\mathscr{E} = -\frac{q}{\epsilon} N_a \int_{-x_{p0}}^{0} dx, \quad -x_{p0} < x < 0 \qquad \text{----------(1.22b)}$$

Therefore, the maximum value of the electric field is

$$\mathscr{E}_0 = -\frac{q}{\epsilon} N_d x_{n0} = -\frac{q}{\epsilon} N_a x_{p0} \qquad \text{---------- (1.23)}$$

- It is simple to relate the electric field $\mathscr{E}$ to the contact potential V_0, since thefield $\mathscr{E}$ at any x is the negative of the potential gradient at that point.

$$\mathscr{E}(x) = -\frac{dV(x)}{dx} \quad \text{or} \quad -V_0 = \int_{-x_{p0}}^{x_{n0}} \mathscr{E}(x) dx \qquad \text{---------- (1.24)}$$

- Thus the negative of the contact potential is simply the area under the $\mathscr{E}(x)$vs. x triangle. This relates the contact potential to the width of the depletion region:

$$V_0 = -\frac{1}{2}\mathscr{E}_0 W = \frac{1}{2}\frac{q}{\epsilon} N_d x_{n0} W \qquad \text{---------- (1.25)}$$

- Since the balance of charge requirement is $x_{n0}.N_d = x_{p0}.Na$, and $W = x_{p0} + x_{n0}$. we can write $x_{n0} = WN_a/(N_a + N_d)$ and substituted in Eq. (1.25).

$$V_0 = \frac{1}{2}\frac{q}{\epsilon}\frac{N_a N_d}{N_a + N_d}W^2 \qquad \text{---------- (1.26)}$$

- By solving for W, in terms of the contact potential, the doping concentrations, and known constants q and ε

$$W = \left[\frac{2\epsilon V_0}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2} = \left[\frac{2\epsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2} \qquad \text{---------- (1.27)}$$

V_0 can be written in terms of the doping concentrations, hence,

$$W = \left[\frac{2\epsilon kT}{q^2}\left(\ln\frac{N_a N_d}{n_i^2}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2} \qquad \text{---------- (1.28)}$$

- The penetration of the transition region into the n and p materials is :

$$x_{p0} = \frac{WN_d}{N_a + N_d} = \frac{W}{1 + N_a/N_d} = \left\{\frac{2\epsilon V_0}{q}\left[\frac{N_d}{N_a(N_a + N_d)}\right]\right\}^{1/2} \qquad \text{-------(1.29a)}$$

$$x_{n0} = \frac{WN_a}{N_a + N_d} = \frac{W}{1 + N_d/N_a} = \left\{\frac{2\epsilon V_0}{q}\left[\frac{N_a}{N_d(N_a + N_d)}\right]\right\}^{1/2} \qquad \text{-------(1.29b)}$$

1.3 Forward & Reverse Biased Junctions

1.3.1 Steady State Conditions

- The feature of a p-n junction is that the current flows in the p to n direction when the p region has a positive external voltage bias with respect to n (forward bias and forward current), whereas no current flows when p is made negative with respect to n (reverse bias and reverse current).
- This asymmetry of the current flow makes the p-n junction diode very useful as a *rectifier*. Biased p-n junctions can be used as voltage-variable capacitors, photocells, light emitters, and many more devices which are basic to modern electronics.

Qualitative Description of Current Flow at a Junction

- If an applied bias voltage V appears across the transition region of the junction rather than in the neutral n and p regions, there will be some voltage drop in the neutral material, if a current flows through it.

- The electrostatic potential barrier at the junction is lowered by the forward bias*(V* = V_f) from the equilibrium contact potential V_0, i.e. to (V_0-V_f). This lowering of the potential barrier occurs because a forward bias raises the electrostatic potential on the p-side with respect to the n-side. For a reverse bias *(V = —Vr)* the opposite occurs; the electrostatic potential of the p side drops with respect to the n side, and the potential barrier at the junction becomes larger *(V_0 + Vr)* as shown in fig. 1.4.
- The electric field within the transition region can be decreased with forward bias, since the applied electric field opposes the built-in field. With reverse bias the field at the junction is increased by the applied field, which is in the same direction as the equilibrium field.
- The change in electric field at the junction changes the transition region width W. Hence the width W will decrease under forward bias (smaller $\mathscr{E}$, fewer uncompensated charges) and will increase under reverse bias.

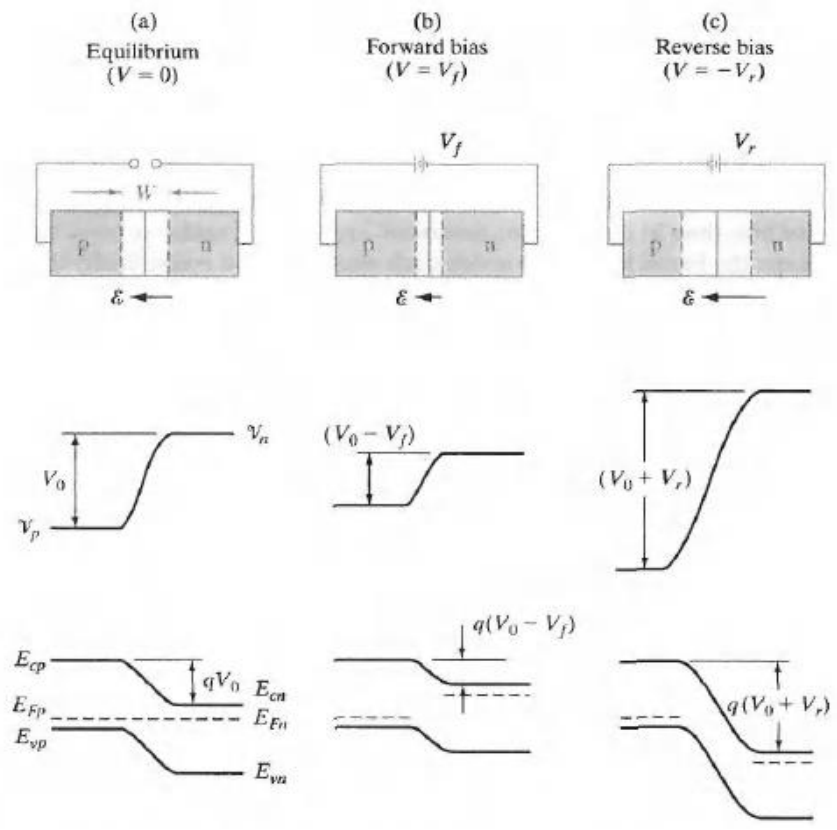


Fig. 1.4: Effect of bias at a p-n junction; transition region width and electric field, electrostatic potential and energy band diagram within *W* for (a) equilibrium, (b) forward bias, and (c) reverse bias.

- The separation of the energy bands is a direct function of the electrostatic potential barrier at the junction. The height of the electron energy barrier is simply the electronic charge q times the height of the electrostatic potential barrier. Thus the bands are separated less [$q(V_0–V_f)$] under forward bias than at equilibrium, and more [$q(V_0 + V_r)$] under reverse bias.
- The shifting of the energy bands under bias implies a separation of the Fermi levels on either side of the junction. Under forward bias, the Fermi level on the n side E_{Fn} is above E_{Fp} by the energy qV_f; for reverse bias, E_{Fp} is qV_r joules higher than E_{Fn}
- The **diffusion current** is composed of majority carriers, electrons on the n-side overcomes the potential energy barrier to diffuse to the p-side, and holes overcomes their barrier from p to n due to **concentration gradient** (rate of change of charge carriers w.r. to distance). With forward bias, the barrier is lowered to (V_0 - V_f), and many more electrons in the n-side conduction band have sufficient energy to diffuse from n to p. Therefore, the electron diffusion current can be quite large with forward bias. Similarly, more holes can diffuse from p to n under forward bias because of the lowered barrier.
- For reverse bias the barrier becomes so large ($V_0 + V_r$) that virtually no electrons in the n-side conduction band or holes in the p-side valence band have enough energy to overcome it. Therefore, the diffusion current is usually negligible for reverse bias.
- The **drift current** is relatively insensitive to the height of the potential barrier and drift current is simply proportional to the applied field.
- The supply of minority carriers on each side of the junction required to participate in the drift component of current is generated by thermal excitation of electron-hole pairs and independent of applied voltage.
- The total current crossing the junction is the sum of the diffusion and drift current components. The net current crossing the junction is zero at equilibrium, since the drift and diffusion components cancel for each type of carriers.

$$I = I(\text{diff.}) - |I(\text{gen.})| = 0 \quad \text{for } V = 0 \qquad \text{--------- (1.30)}$$

- Under reverse bias, both diffusion components are negligible because of the large barrier at the junction, and relatively small (and essentially voltage-independent)

generation current from n to p. This generation current is shown in Fig. 1.5, in a sketch of a typical *I- V* plot for a p-n junction.

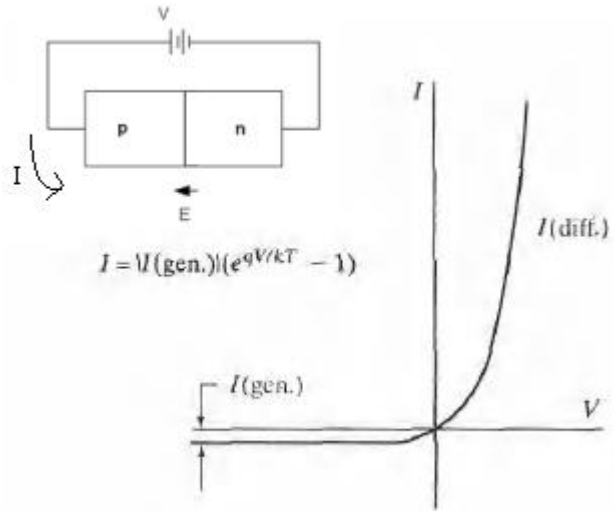


Fig. 1.5: I-V characteristics of a p-n junction.

- An applied forward bias V = V_f increases the probability that a carrier can diffuse across the junction, by the factor *exp(qV/kT).* Thus the diffusion current under forward bias is given byits equilibrium value multiplied by *exp(qV/kT);* similarly, for reverse bias (with V = -Vr) the diffusion current is the equilibrium value reduced by the same factor.
- The total current **I** is then the diffusion current minus the absolute value of the generation current, I_0. From Eq. (1.30),

$$I = I_0(e^{qV/kT} - 1) \qquad \text{---------- (1.31)}$$

- In Eq. (1.31) the applied voltage V is positive (forward bias) and greater than a few kT/q, the exponential term is much greater than unity. The current thus increases exponentially with forward bias. When V is negative (reverse bias), the exponential term approaches zero and the current is **$-I_0$**, which is in the n to p (negative) direction. This negative generation current is also called the **reverse saturation current**.

Carrier Injection

- The minority carrier concentration on each side of a p-n junction varies with the applied bias because of variations in the diffusion of carriers across the junction. The equilibrium ratio of hole concentrations on each side are;

$$\frac{p_p}{p_n} = e^{qV_0/kT} \qquad \text{--------- (1.32)}$$

$$\frac{p(-x_{p0})}{p(x_{n0})} = e^{q(V_0-V)/kT} \qquad \text{--------- (1.33)}$$

- This equation uses the altered barrier (V_0–V) to relate the steady state hole concentrations on the two sides of the transition region with either forward or reverse bias.With this simplification we can write the ratio of above two equations as:

$$\frac{p(x_{n0})}{p_n} = e^{qV/kT} \quad \text{taking } p(-x_{p0}) = p_p \qquad \text{---------- (1.34)}$$

- The excess hole concentration Δp_n at the edge of the transition region x_{n0} is obtained by subtracting the equilibrium hole concentration from Eq. (1.34),

$$\boxed{\Delta p_n = p(x_{n0}) - p_n = p_n(e^{qV/kT} - 1)} \qquad \text{---------- (1.35)}$$

and similarly for excess electrons on the p side,

$$\boxed{\Delta n_p = n(-x_{p0}) - n_p = n_p(e^{qV/kT} - 1)} \qquad \text{---------- (1.36)}$$

- For convenience, let us define two new coordinates: Distances measured in the x-direction in the n material from x_{n0} will be designated x_n; distances in the p material measured in the -x-direction with -x_{p0} will be designated as x_p.
- Consider the diffusion equation for each side of the junction and solve for the distributions of excess carriers *(δn* and *δp)* assuming long p and n regions:

$$\boxed{\delta n(x_p) = \Delta n_p e^{-x_p/L_n} = n_p(e^{qV/kT} - 1)e^{-x_p/L_n}} \qquad \text{---------- (1.36a)}$$

$$\boxed{\delta p(x_n) = \Delta p_n e^{-x_n/L_p} = p_n(e^{qV/kT} - 1)e^{-x_n/L_p}} \qquad \text{---------- (1.36b)}$$

- The hole diffusion current at any point x_n in the n material is

$$I_p(x_n) = -qAD_p\frac{d\delta p(x_n)}{dx_n} = qA\frac{D_p}{L_p}\Delta p_n e^{-x_n/L_p} = qA\frac{D_p}{L_p}\delta p(x_n) \qquad \text{---------- (1.37)}$$

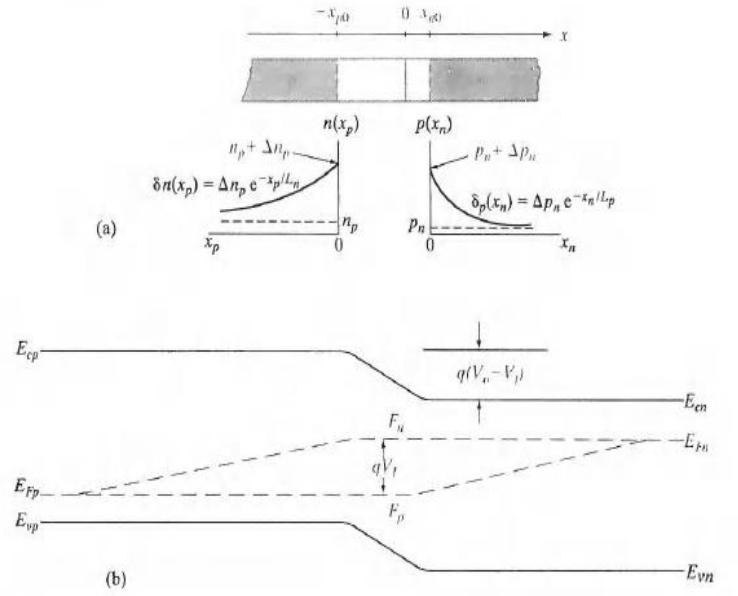


Fig. 1.6: Forward-biased junction: (a) minority carrier distributions on the two sides of the transition region and definitions of distances x_n and x_p measured from the transition region edges; (b) variation of the quasi-Fermi levels with position.

- The total hole current injected into the n material at the junction can be obtained simply by evaluating above equation at x_n=0

$$I_p(x_n = 0) = \frac{qAD_p}{L_p}\Delta p_n = \frac{qAD_p}{L_p}p_n(e^{qV/kT} - 1) \qquad \text{---------- (1.38)}$$

$$I_n(x_p = 0) = -\frac{qAD_n}{L_n}\Delta n_p = -\frac{qAD_n}{L_n}n_p(e^{qV/kT} - 1) \qquad \text{---------- (1.39)}$$

$$I = I_p(x_n = 0) - I_n(x_p = 0) = \frac{qAD_p}{L_p}\Delta p_n + \frac{qAD_n}{L_n}\Delta n_p \qquad \text{-------- 1.40}$$

$$\boxed{I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)(e^{qV/kT} - 1) = I_0(e^{qV/kT} - 1)} \qquad \text{------ 1.41}$$

- Eq. (1.41) is the ***diode equation***, describes the total current through the diode for either forward or reverse bias.

- The current for reverse bias is calculated by letting $V = -V_r$:

$$I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)(e^{-qV_r/kT} - 1) \qquad \text{-------- (1.42)}$$

- If V_r is larger than a few kT/q, the total current is just the reverse saturation current

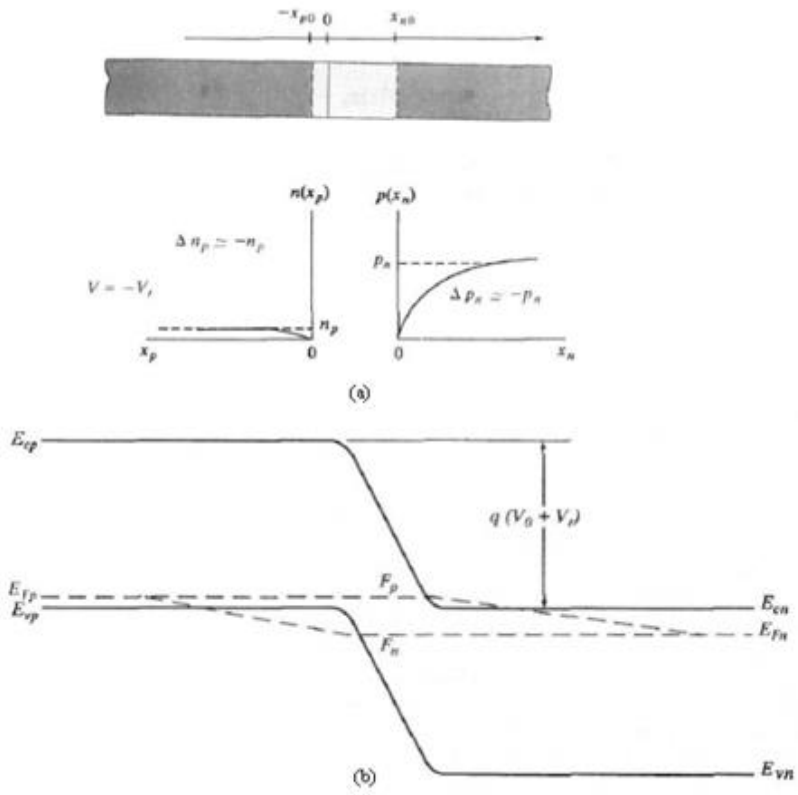
$$I = -qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right) = -I_0 \qquad \text{---------- (1.43)}$$

Reverse Bias

- The distributions of carriers for reverse bias is,

$$\Delta p_n = p_n(e^{q(-V_r)/kT} - 1) \simeq -p_n \quad \text{for } V_r \gg kT/q \qquad \text{-------- (1.44)}$$

- Thus for a reverse bias of more than a few tenths of a volt, the minority carrier concentrations at each edge of the transition region becomes essentially zero as the excess concentration approaches the negative of the equilibrium concentration.



- **Fig. 1.7: Reverse biased P-N junction (a) minority carrier distributions near the reverse-biased junction; (b) variation of the quasi-Fermi levels.**

- This reverse-bias depletion of minority carriers can be thought of as minority carrier extraction, analogous to the injection of forward bias.
- For example, when holes at x_{n0} are swept across the junction to the p side by thefield $\mathscr{E}$, a gradient in the hole distribution in the n material exists, and holes in the n region diffuse toward the junction.
- The rate of carrier drift across the junction (reverse saturation current) depends on the rate at which holes arrive at x_{n0} (and electrons at x_{p0}) by diffusion from the neutral material. These minority carriers are supplied by thermal generation.
- The F_n moves farther away from E_c(close to E_v) and F_p moves farther away from E_v. In reverse bias, in the depletion region, we have

$$pn = n_i^2 e^{(F_n - F_p)/kT} \approx 0 \qquad \text{------- (1.45)}$$

1.4Reverse Bias Breakdown

- When the P-N junction diode operates in reverse bias, a very small amount of saturation current flows .This current flows until a critical reverse bias is reached ($\mathbf{V_{br}}$). At this value of critical voltage ($\mathbf{V_{br}}$) the reverse saturation current through the diode increases sharply.

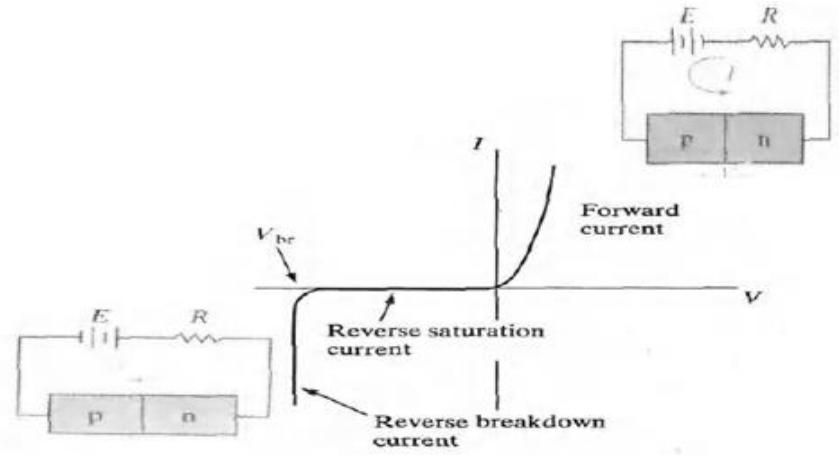


Fig. 1.9: Reverse breakdown in a p-n junction

- Relatively large currents can flow with further increase in voltage. If the current in reverse bias is limited to a reasonable value by the external circuit, the P-N junction can be operated in safe-mode (not in break-down).

- The maximum reverse current that can flow in the device is $(E - V_{br}) / R$, where, E = applied reverse voltage, V_{br} = break down voltage, and R = series resistance (to limit the current).
- R can be chosen to limit the current to a safe level. If the current is not limited externally, the P-N junction can be damaged by excessive reverse current.
- Reverse break down can occur by two mechanisms
  - Zener breakdown
  - Avalanche breakdown
- Both the break down mechanisms requires a critical electric field.
- If the break-down occur at low voltages (up to a few volts reverse bias), the mechanism is **zener breakdown**.
- If the break-down occur at higher voltages (from a few volts to thousands of volts), the mechanism is **avalanche breakdown**.

1.4.1 Zener Breakdown

- It is due to field ionization. This break down mechanism follows the tunneling phenomenon. Zener effect is due to **field ionization** of the atoms at the junction.
- **Zener effect:** When a heavily doped junction is reversebiased, the energy bands become crossed at relatively low voltages i.e, n- side conduction appears opposite the p – side valance band.If the barrier separating these two bands is narrow, tunneling of electrons from p–side valence band to n-side conduction band can occur.This tunneling of electrons from p-side to n-side constitutes a reverse current from n to p, called the zener effect.
- Basic requirement for the tunneling current is narrow barrier of finite height.
- Since the tunneling probability depends upon the width of the barrier, it is important that the junction must be sharp and must be heavily doped, so that the transition region W extends only a very short distance from each side of the junction.
- Reverse bias of a heavily doped junction causes a large electric field with in space charge region‘W’.As reverse bias increases, electric field within ‘W’ increases, tunneling distance, ‘d’ becomes smaller.

- At one value of field strength (critical field strength), electrons participating in covalent bonds may come out from the bonds by the field and accelerated to the n-side of the junction. Electric field of 10^6 V/cm is required for this type of ionization.

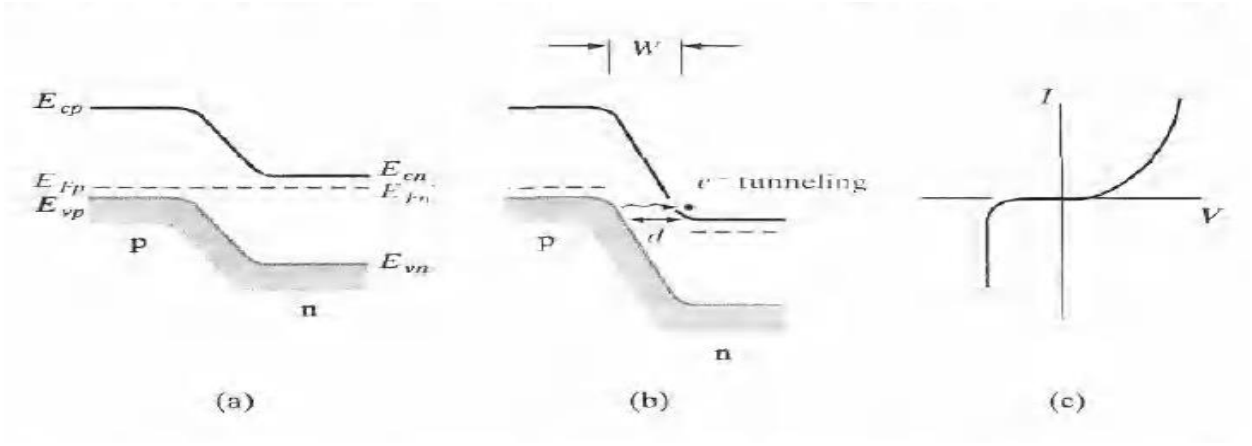


Fig. 1.9: The Zener effect: (a) heavily doped junction at equilibrium; (b) reverse bias with electron tunneling from p to n; (c) l-V characteristic.

1.4.2 Avalanche Breakdown

- If the electric field $\mathscr{E}$ in the transition region is large, an electron entering from the p-side may be accelerated to high enough kinetic energy to cause an ionizing collision with lattice.
- A single such interaction results in *carrier multiplication*; the original electron and generated electron are both swept to the n-side of the junction and the generated hole is swept to the p-side.
- The degree of multiplication can become very high if the carriers generated within the transition region also have ionizing collisions with lattice. This is called *avalanche process.*
- For n_{in} electrons entering from p-side, there will be Pn_{in} ionizing collisions and EHP (secondary carriers) for each collision.
- After Pn_{in} collisions by the primary electrons, we have the primary plus the secondary electrons n_{in} (1+P)
- For $n_{in}P$ secondary pairs there will be ($n_{in}P$) P ionizing collisions and $n_{in}P^2$ tertiary pairs.
- Summing up the total number of electrons out of the region at n after many collisions,

$$n_{out} = n_{in}(1+ P + P^2 + P^3 + - - - - - - - - - -)$$ ---------- **(1.46)**

- Electron multiplication is

$$M_n = \frac{n_{out}}{n_{in}} = 1 + P + P^2 + P^3 + \cdots = \frac{1}{1 - P}$$ ---------- (1.43 a)

$$M = \frac{1}{1 - (V/V_{br})^n}$$ ---------- (1.43 b)

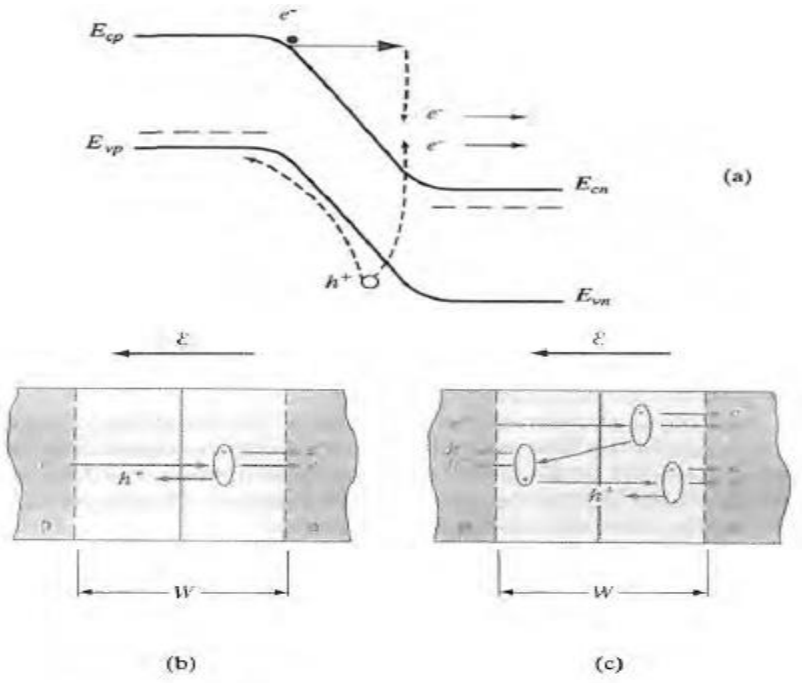


Fig. 1.10: Electron-hole pairs created by impact ionization: (a) band diagram of a p-n junction in reverse bias; (b) A single ionizing collision by an incoming electron in the depletion region of the junction; (c) Primary, secondary, and tertiary collisions.

1.5 The Ideal Diode

- An ideal diode is a diode that acts like a perfect conductor when voltage is applied forward biased and like a perfect insulator when voltage is applied reverse biased.
- So when positive voltage is applied across the anode to the cathode, the diode conducts forward current instantly. When voltage is applied in reverse, the diode conducts no current at all.
- The Ideal Diode may be considered the most fundamental nonlinear circuit element.

1.5.1 Current-Voltage Characteristics

- The terminal characteristic of the ideal diode can be interpreted as follows:
- If a negative voltage is applied to the diode, no current flows and the diode behave like an open circuit. Diodes operated in this mode are said to be reverse biased,. An ideal diode has zero current when operated in reverse direction and is said to be cut off, or simply off.
- If a positive current is applied to the ideal diode, zero voltage drop appears across the diode. The ideal diode behaves as a short circuit in the forward direction; it passes any current with zero voltage drop. A forward biased diode is said to be **turned on**, or simply **on**.

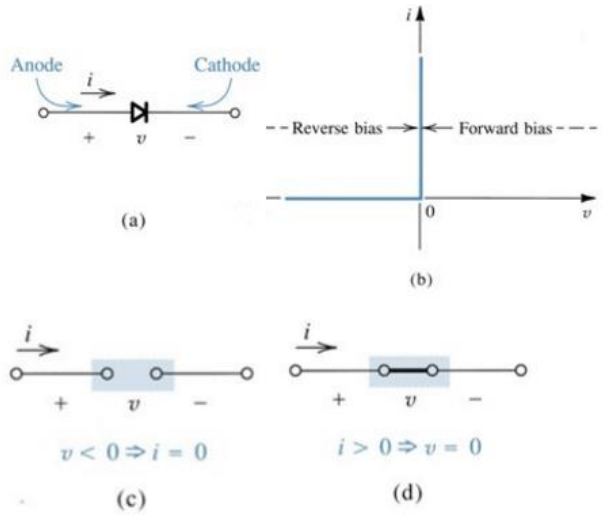


Fig. 1.11: Ideal diode: (a) diode circuit symbol; (b) *i-v* characteristics; (c) equivalent circuit in reverse direction; (d) equivalent circuit in forward direction

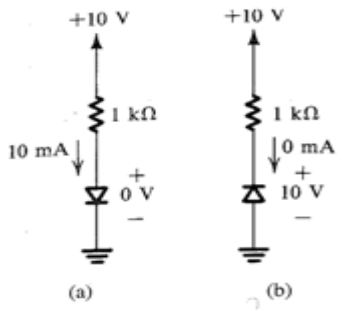


Fig. 1.12: The two modes of operation of ideal diodes and the use of an external circuit to limit (a) the forward current and (b) the reverse voltage

1.6 Terminal Characteristics of Junction Diodes

- The characteristic curve consists of three distinct regions:
  - The forward-bias region, determined by v>0
  - The reverse-bias region , determined by v>0
  - The breakdown region, determined by v< -V_{zk}
- These three regions of operation are described in the following sections.

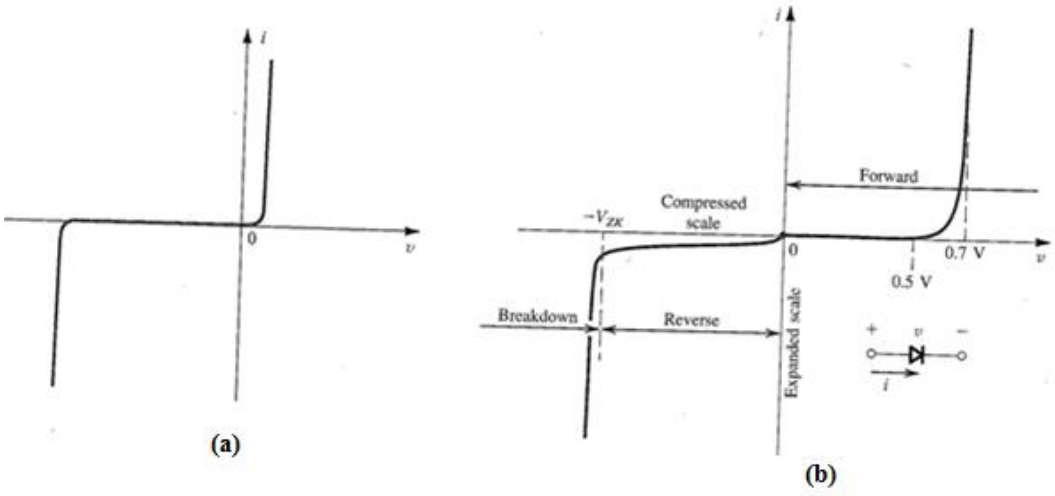


Fig. 1.13: (a) The *i-v* characteristics of silicon diode (b) The diode *i-v* relationship with some scales

1.6.1 The Forward-Bias Region

- The forward-bias of operation is entered when the terminal voltage V is positive.
- In the forward region the *i-v* relationship is closely approximated by

$$i = Is\ (e^{V/\eta V_T} - 1)$$

- In this equation, *Is* is constant for a given diode at a given temperature and is usually called as the saturation current. Another name which is occasionally used is scale current. Is is directly proportional to the cross-sectional area of the diode.
- For small-signal diodes, *Is* is of the order of 10-15 A. It doubles in value for every 5^oC rise in temperature.
- The voltage V_T is a constant called the thermal voltage and is given by

$$V_T = kT/q$$

Where, k = Boltzmann's constant = $1.38 * 10^{-23}$ joules/kelvin

T = the absolute temperature in kelvins = 273 + temperature in ^oC

q = the magnitude of electronic charge = $1.60 * 10^{-19}$ coulomb

- At room temperature the value of V_T is 25.2mV. Approximately we shall use VT= 25mV in circuit analysis.
- The constant n in diode equation has a value between 1 and 2, depending on the material and physical structure of the diode.
- For appereciable current in the forward direction, specifically for i >>Is, the equation for i can be approximated as

$$i = I_S.e^{V/\eta V_T}$$

This relationship can be expressed alternatively in the logarithmic form as

$$V = \eta V_T \ln (i/I_S)$$

Let us evaluate current i_1 corresponding to a diode voltage V_1:

$$i_1 = I_S. e^{V_1/\eta V_T}$$

Similarly, if the voltage is V_2 , the diode current I_2 will be

$$i_2 = I_S e^{V_2/\eta V_T}$$

These two equations can be combined to produce

$$i_2/i_1 = e^{(V_2-V_1)/ \eta V_T}$$

which can be re written as

$$V_2 - V_1 = \eta V_T.\ln (I_2/I_1) \text{ or } V_2 - V_1 = 2.3\eta V_T.\log (I_2/I_1)$$

- This equation states that for a decade change in current, the diode voltage drop changes by $2.3\eta V_T$.
- The *i-v* characteristics in the forward region reveal that the current is negligibly small for V smaller than about 0.5V. This value is usually referred to as the cut-in voltage.

1.6.2 The Reverse - Bias Region

- The reverse-bias region of the operation is entered when the diode voltage v is made negative.
- Equation predicts that if v is negative and a few times larger than V_T(25mV) in magnitude, the exponential term becomes negligibly small compared to unity, and the diode current becomes

$$i = -I_S$$

- That is, the current in the reverse direction is constant and equal to I_S. This constancy is the reason behind the term saturation current.
- Real diodes exhibit reverse currents that, though quite small, are much larger than I_S.
- A large part of the reverse current is due to leakage effects. These leakage currents are proportional to junction area. Temperature dependence of the reverse current doubles for every 10^oC rise in temperature.

1.6.3 The Breakdown Region

- The breakdown region is entered when magnitude of the reverse voltage exceeds a threshold value of a particular diode, called the Breakdown Voltage.
- This is the voltage at the "knee" of the *i-v* curve and is denoted as V_{ZK}, where, z stands for zener and k stands for knee.
- In the breakdown region the reverse current increases rapidly, with the associated increase in voltage drop being very small.
- It is necessary to limit the reverse current in the breakdown region t value consistent with the permissible power dissipation.
- The diode i-v characteristics in breakdown are almost a vertical line which enables it to be used in voltage regulation.

1.7 Metal-Semiconductor Junctions

- Metal–semiconductor junction is a type of junction in which a metal comes in close contact with a semiconductor material.

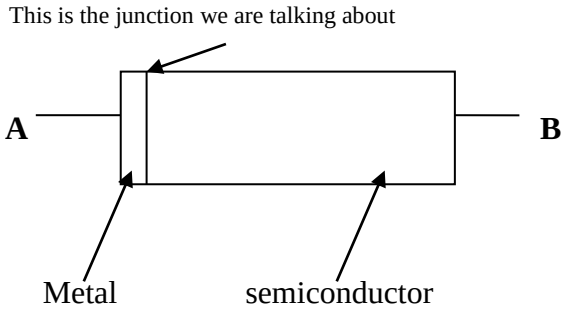


Fig. 1.14 Metal–semiconductor junction

- Many of useful properties of a P-N junction can be achieved by forming metal-semiconductor contact.
- Comparison of metal-semiconductor and p-n junctions are

- There is no minority carrier injection, it is a majority carrier device, (modulation and switching can be much faster)
- The metal-semiconductor junction current is higher at the same bias (metal-semiconductor barrier is always lower)

➢ There are 2 kinds of metal-semiconductor contacts

i) Rectifying contacts (schottky barrier) - *metal on lightly doped silicon*

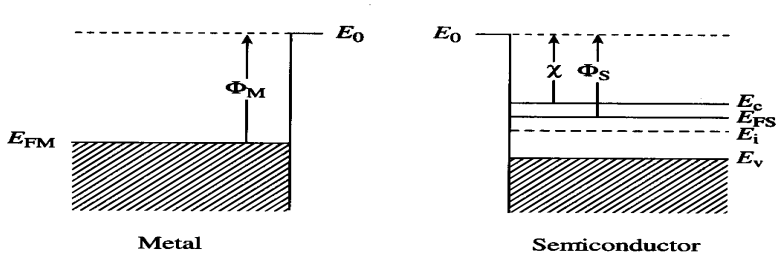
ii) Ohmic contacts (low resistance non-rectifying) - *metal on heavily doped silicon*

Schottky Barrier

➢ Schottky barrier is formed by contacting a N-type or P-type semiconductor with a metal.

➢ The quantity ϕ (volts) is the characteristic of the particular metal or semiconductor.

➢ **Work Function:** The energy qϕ is called the work function, which represents the minimum energy required for an electron to escape from (Fermi level) metal into vacuum.



(a) Metal band diagram **(b) Semiconductor band diagram**

Fig. 1.15: Difference between metal & semiconductor band diagrams

Where, ϕ_m - metal work function and ϕ_s– semiconductor work function

➢ **Schottky Effect:** When negative charges are brought near the metal surface, positive (image) charges are induced in metal. When this image force is combined with an applied electric field, the effective work function is somewhat reduced. Such barrier lowering is called the Schottky effect.

1.7.1 Metal - Semiconductor Before Joining

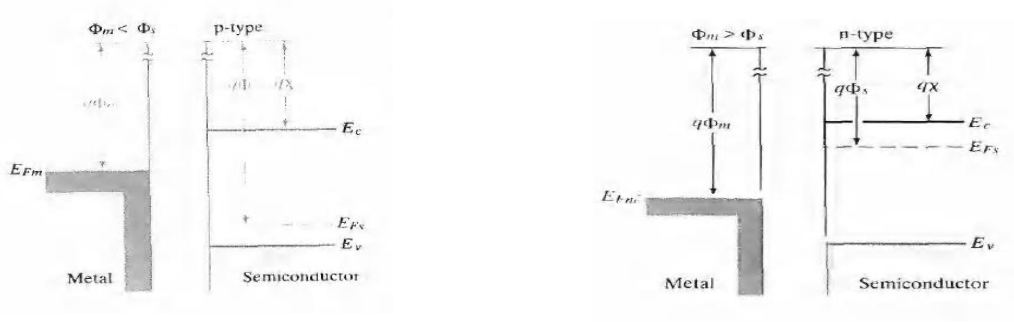


Fig. 1.16: Band diagrams for the metal - semiconductor before joining: (a) p-type semiconductor with a metal, (b) n-type semiconductor with a metal

- $\phi_m < \phi_s$ - Metal Fermi level is higher than that of the P -type semiconductor
- $\phi_m > \phi_s$ - Semiconductor fermi level is higher than that of the metal
- Electron affinity ($q\chi$) : which is measured from the vacuum level to the conduction band edge.

1.7.2 Metal - Semiconductor at Equilibrium (zero bias): When a metal with work function $q\phi_m$ is brought in contact with a semiconductor having a work function $q\phi_s$ charge transfer occurs until the Fermi levels align at equilibrium

- **$\phi_m > \phi_s$ condition :**

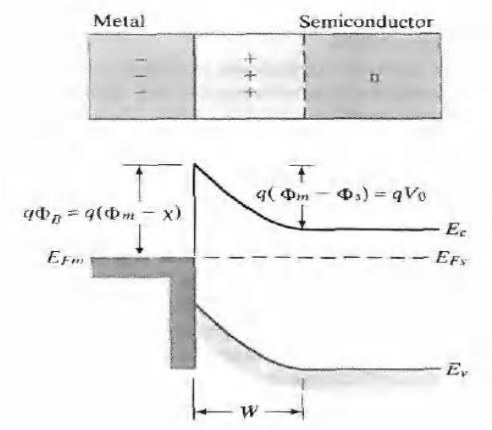


Fig. 1.17: Equilibrium Band diagram of a metal – N-type semiconductor contact

✓ To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (i.e., the electron energies must be lowered) relative to that of the metal.

- ✓ In the n-type semiconductor as shown in Fig 1.19 depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal.
- ✓ The equilibrium contact potential Vo, which prevents further net electron diffusion from the semiconductor conduction band into the metal, is the difference in work function potentials $\phi_m - \phi_s$.
- ✓ The potential barrier height ϕ_B for electron injection from the metal into the semiconductor conduction band is $\phi_m - \chi$.

1.7.3 $\phi_m < \phi_s$ condition:

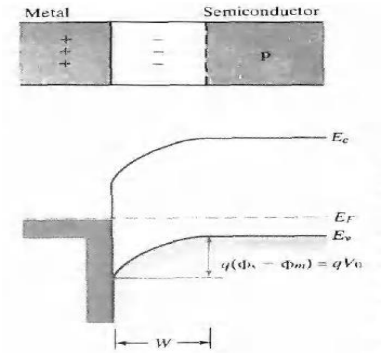


Fig. 1.18: Equilibrium Band diagram of a metal – P-type semiconductor contact

- ✓ To align the Fermi levels at equilibrium requires a positive charge on the metal side and a negative charge on the semiconductor side of the junction.
- ✓ The negative charge is accommodated by a depletion region W in which ionized acceptors (Na^-) are left uncompensated by holes.
- ✓ The potential barrier V_0 retarding hole diffusion from the semiconductor to the metal is $\phi_s - \phi_m$.

1.7.4 Rectifying Contacts

- ➢ A rectifying contact only allows current to flow one way, with an I-V curve that looks a lot like a diode - in fact, it's usually referred to as a Schottky diode.

  Case -1: Schottky barrier (Metal-N type semiconductor)

  - **Forward-bias voltage, *V*** is applied to the Schottky barrier (metal-N-type semiconductor): Due to forward bias contact potential is reduced from V_0 to V_0 - V. As a result, electrons in the semiconductor conduction band can diffuse across the

depletionregion to the metal. This gives rise to a forward current (metal to semiconductor) through the junction.

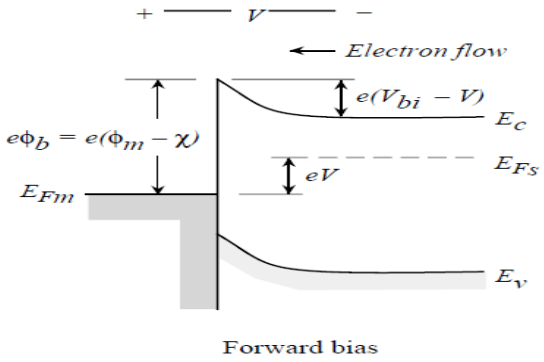


Fig. 1.19: Effects of forward bias on the junction

- **Reverse-bias voltage, *V*** is applied to the Schottky barrier (metal-N type semiconductor): Reverse bias increases the barrier voltage V_o to $V_o + Vr$, and electron flow from semiconductor to metal (becomes negligible.)

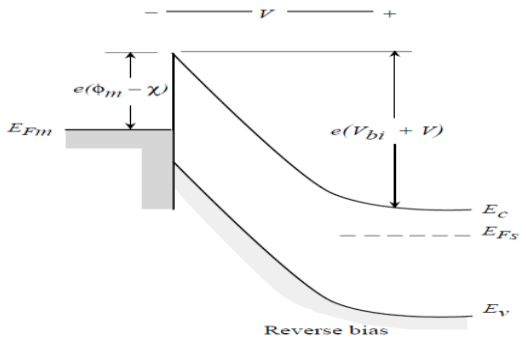


Fig. 1.20: Effects of Reverse bias on the junction

- **I –V Characteristics**

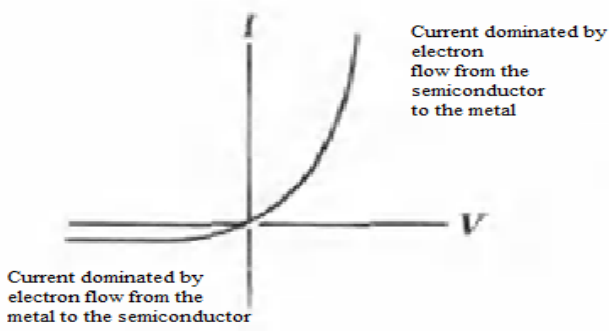


Fig. 1.21: Typical Current-Voltage Characteristics

✓ In either case flow of electrons from the metal to the semiconductor is retarded by the barrier $\phi_m - \chi$.

- ✓ The resulting diode current equation is similar in form to that of the p-n junction

$$\mathbf{I = I_0 (e^{qv/k\,T}-1)}$$

- ✓ The saturation current should depend upon the size of the barrier ϕ_B for electron injection from the metal into the semiconductor.
- ✓ Barrier (which is $\phi_w - \chi$ for the ideal case) is unaffected by the bias voltage.

$$\mathbf{I_0 \ \alpha \ e^{-q\phi_B/kT}}$$

Case-2: Schottky barrier (Metal- P type semiconductor)

- The diode equation can also applied to the metal-p-type semiconductor junction. In this case forward voltage (the semiconductor biased positively with respect to the metal) increases the forward current as this voltage lowers the potential barrier V_0 to $V_0 - V$ and holes flow from the semiconductor to the metal. Of course, a reverse voltage increases the barrier for hole flow and the current becomes negligible.

➢ **Rectifying contact Conclusion**

- In both the cases the Schottky barrier is rectifying, with easy current flow in the forward direction and little current in the reverse direction.
- We can also note that the forward current in any case is due to injection of majority carriers from the semiconductor into the metal or metal into the semiconductor.
- The absence of minority carrier injection and the associated storage delay time is an important feature of Schottky barrier diodes.
- Rectifying contacts are less temperature dependent.
- Although some minority carrier injection occurs at high current levels, these are essentially majority carrier devices.
- Their high-frequency properties and switching speed are generally better than typical p-n junctions.Unlike a p-n diode, in forward bias no minority carrier injection occurs. Thus there is no diffusion capacitance and the device response is very fast
- Schottky barrier devices are particularly well suited for use in densely packed integrated circuits, because fewer photolithographic masking steps are required compared to P-N junction devices.
- The cut-in voltage (V_0) is quite small for rectifying contacts.

1.7.5 Ohmic Contacts

- An ohmic contact is a metal-semiconductor junction that allows current to flow both ways roughly equally within normal device operation range.
- A practical method for forming ohmic contacts is by doping the semiconductors heavily in the contact region. Thus the depletion width is small enough to allow carriers to tunnel through the barrier.

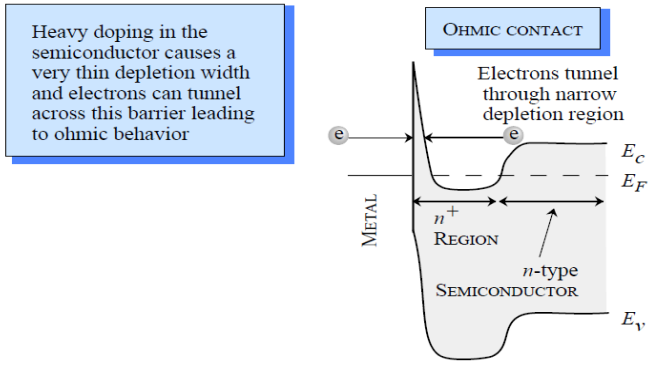


Fig. 1.22: Tunneling phenomenon in Metal - Semiconductors

- With a voltage-current relationship (linear I-V curve) that comes close to that of a resistor, hence the name "ohmic".
- The surface of typical IC is made of P and N regions, which must be contacted & interconnected, those contacts be ohmic.
- Ohmic contacts should have minimal resistance and no tendency to rectifying signal.
  - **$\phi_m < \phi_s$ condition:**

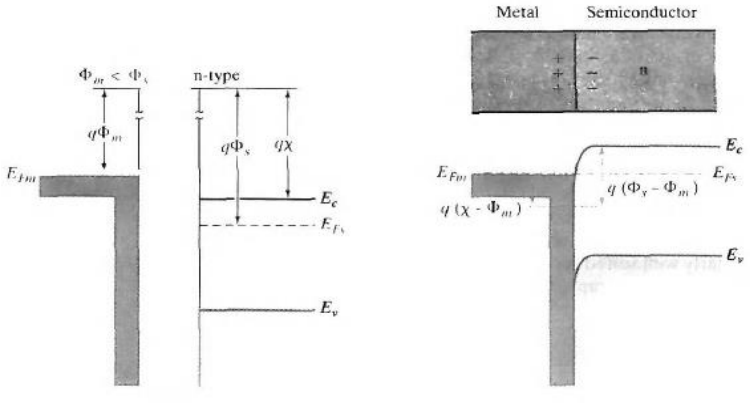


Fig. 1.23: Ohmic metal-semiconductor contacts: (a) $\phi_m < \phi_s$ for an n-type semiconductor, and (b) the equilibrium band diagram for the junction

- ✓ Fermi levels are aligned at equilibrium by transferring electrons from the metal to the semiconductor.
- ✓ This raises the semiconductor electron energies relative to the metal at equilibrium.
- ✓ In this case the barrier becomes small; hence a small amount of voltage is enough to electron flow between metal and semiconductor.

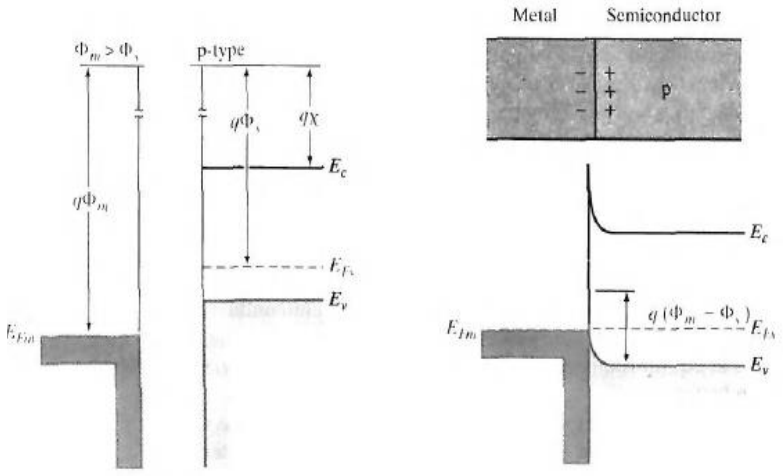


Fig. 1.24: Ohmic metal-semiconductor contacts: (a) $\phi_m > \phi_s$ for an P-type semiconductor, and (b) the equilibrium band diagram for the junction

- ➢ Unlike the rectifying contacts no depletion region occurs in the semiconductor in the ohmic contacts.

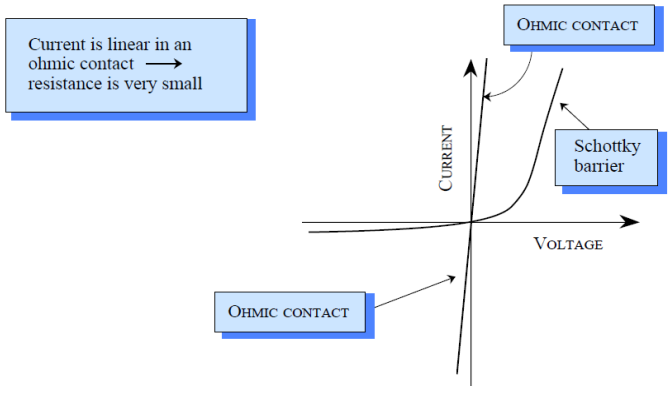


Fig. 1.25: I –V characteristics of Ohmic & Schottky barriers

1.8 The ideal MOS capacitor

- The work function characteristic of the metal can be defined in terms of the energy required to move an electron from the Fermi level to outside the metal.
- In MOS transistors it is more convenient to use a modified work function $q\phi_m$ for the metal-oxide interface. The energy $q\phi_m$ is measured from the metal Fermi level to the conduction band of the oxide. Similarly, $q\phi s$ is the modified work function at the semiconductor-oxide interface. In idealized case we assume that $\phi_m = \phi s$.
- Another quantity that will be useful in later discussions is $q_{\phi F}$, which measures the position of the Fermi level below the intrinsic level E_i for the semiconductor. This quantity indicates how strongly p-type the semiconductor is.
- **Band diagram for the ideal MOS structure at equilibrium**

- The MOS structure of below Fig. 3.15 is essentially a capacitor in which one plate is a semiconductor.

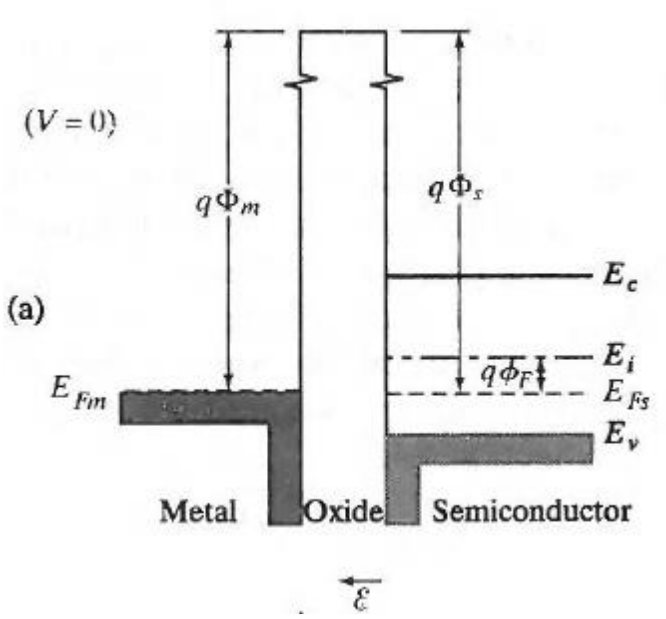


Fig. 1.26 : Band diagram for the ideal MOS structure at: (a) equilibrium;

- **Accumulation**

- If we apply a negative voltage between the metal and the semiconductor, we effectively deposit a negative charge on the metal. In response, we expect an equal net

positive charge to accumulate at the surface of the semiconductor. In the case of a p-type substrate this occurs by *hole accumulation* at the semiconductor-oxide interface.

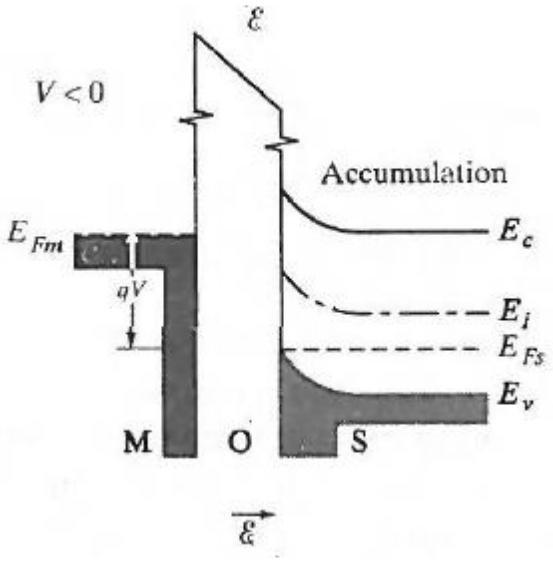


Fig. 1.27: Negative voltage causes hole accumulation in the p-type semiconductor

- Since the applied negative voltage depresses the electrostatic potential of the metal relative to the semiconductor, the electron energies are raised in the metal relative to the semiconductor.
- As a result, the Fermi level for the metal E_{Fm} lies above its equilibrium position by qV, where V is the applied voltage. Since ϕm and ϕs do not change with applied voltage, moving E_{Fm} up in energy relative to EFs causes a tilt in the oxide conduction band.
- We expect such a tilt since an electric field causes a gradient in Ei (and similarly in Evand *Ec)*

$$\mathscr{E}(x) = \frac{1}{q}\frac{dE_i}{dx}$$

- The energy bands of the semiconductor bend near the interface to accommodate the accumulation of holes. Since

$$p = n_i e^{(E_i - E_F)/kT}$$

- It is clear that an increase in hole concentration implies an increase in Ei — EF at the semiconductor surface.

- Since no current passes through the MOS structure, there can be no variation in the Fermi level within the semiconductor. Therefore, if E, - EF is to increase, it must occur by Ei moving up in energy near the surface. The result is a bending of the semiconductor bands near the interface. We notice in above Fig. 3.16 that the Fermi level near the interface lies closer to the valence band, indicating a larger hole concentration than that arising from the doping of the p-type semiconductor.

➢ **Depletion**

- If we apply a positive voltage from the metal to the semiconductor. This raises the potential of the metal, lowering the metal Fermi level by qV relative to its equilibrium position. As a result, the oxide conduction band is again tilted.

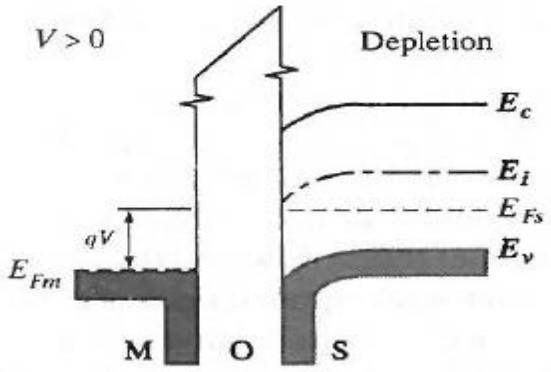


Fig. 1.28: Positive voltage depletes holes from the semiconductor surface

- It is noticed that the slope of this band is obtained by simply moving the metal side down relative to the semiconductor side, is in the proper direction for the applied field.The positive voltage deposits positive charge on the metal and calls for a corresponding net negative charge at the surface of the semiconductor. Such a negative charge in p-type material arises from *depletion* of holes from the region near the surface, leaving behind uncompensated ionized acceptors.

➢ **Inversion**

- If we continue to increase the positive voltage, the bands at the semiconductor surface bend down more strongly. In fact, a sufficiently large voltage can bend E_i *below* E_F as shown in Fig. 1.29.

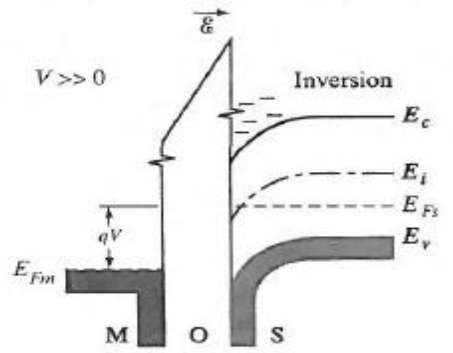


Fig. 1.29: A larger positive voltage causes inversion - an "n type" layer at the semiconductor surface.

- This is a particularly interesting case, since EF >Ei implies a large electron concentration in the conduction band.
- The region near the semiconductor surface in this case has conduction properties of n-type material.
- This n-type surface layer is formed not by doping, but instead by inversion of the originally p-type semiconductor due to the applied voltage.
- This inverted layer, separated from the underlying p-type material by a depletion region, is the key to MOS transistor operation. The inversion region becomes the conducting channel in the FET.

➢ **Overview:** we define a potential ϕ at any point *x*, measured relative to the equilibrium position of E_f. The energy $q\phi$ tells us the extent of band-bending at x, and $q\phi_s$ represents the band-bending at the surface. We notice that

- ✓ ϕs= 0 is the ***flat band*** **condition** for this ideal MOS case (i.e., the bands look like Fig. 1.26)
- ✓ When ϕ_s<0, the bands bend up at the surface, and we have **hole accumulation** ((i.e., the bands look like Fig. 1.27)
- ✓ When ϕ_S> 0, we have **depletion** (i.e., the bands look like Fig. 1.28)
- ✓ When ϕ_s is positive and larger than ϕ_F, the bands at the surface are bent down such that Ei(x = 0) lies below E_F, and **inversion** is obtained (i.e., the bands look like Fig. 1.29)

- The best criterion for *strong inversion* is that the surface should be as strongly n-type as the substrate is p-type. That is, *Ei* should lie as far below $E_F$at the surface as it is above *EF* far from the surface.
- This condition occurs when

$$\phi_s(\text{inv.}) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$

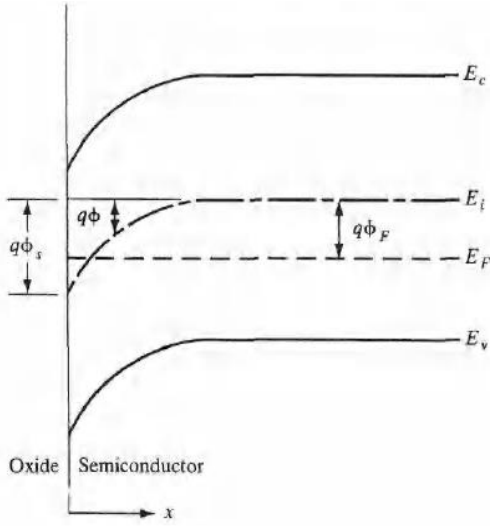


Fig. 1.30 : Bending of the semiconductor bands at the onset of strong inversion: the surface potential ϕ_s is twice the value of ϕ_F in the neutral p material

- A surface potential of <$>*F* is required to bend the bands down to the intrinsic condition at the surface $E_i = E_F$), and *Ei* must then be depressed another $q\phi_F$ at the surface to obtain the condition we call strong inversion.
- The electron and hole concentrations are related to the potential $\phi(x)$. Since the equilibrium electron concentration is

$$n_0 = n_i e^{(E_F - E_i)/kT} = n_i e^{-q\phi_F/kT}$$

- we can easily relate the electron concentration at any *x* to this value:

$$n = n_i e^{-q(\phi_F - \phi)/kT} = n_0 e^{q\phi/kT}$$

and similarly for holes:

$$p_0 = n_i e^{q\phi_F/kT}$$
$$p = p_0 e^{-q\phi/kT}$$

- At any *x,* we could combine these equations with Poisson's equation and the usual charge density expression to solve for $\boldsymbol{\phi}(x)$.Poisson's equations are

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_s}$$
$$\rho(x) = q(N_d^+ - N_a^- + p - n)$$

- Let us solve this equation to determine the total integrated charge per unit area, Q_s ,as a function of the surface potential, ϕs. By Substituting the Equations, we get

$$\frac{\partial^2 \phi}{\partial x^2} = \frac{\partial}{\partial x}\left(\frac{\partial \phi}{\partial x}\right) = -\frac{q}{\epsilon_s}\left[p_0\left(e^{-\frac{q\phi}{kT}} - 1\right) - n_0\left(e^{\frac{q\phi}{kT}} - 1\right)\right]$$

- It should be kept in mind that

$$\frac{-\partial \phi}{\partial x}$$

is the electric field, E, at a depth *x.* Integrating above Equation from the bulk (where the bands are flat, the electric fields are zero, and the carrier concentrations are determined solely by the doping), towards the surface, we get

$$\int_0^{\frac{\partial \phi}{\partial x}} \left(\frac{\partial \phi}{\partial x}\right) d\left(\frac{\partial \phi}{\partial x}\right) = -\frac{q}{\epsilon_s}\int_0^{\phi}\left[p_0\left(e^{\frac{-q\phi}{kT}} - 1\right) - n_0\left(e^{\frac{q\phi}{kT}} - 1\right)\right] d\phi$$

- After integration, we then get

$$\mathscr{E}^2 = \left(\frac{2kT\, p_0}{\epsilon_s}\right)\left[\left(e^{\frac{-q\phi}{kT}} + \frac{q\phi}{kT} - 1\right) + \frac{n_0}{p_0}\left(e^{\frac{q\phi}{kT}} - \frac{q\phi}{kT} - 1\right)\right]$$

- A particularly important case is at the surface *(x* = 0) where the surface perpendicular electric field, *Es,* becomes

$$\mathscr{E}_s = \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\frac{q\phi_s}{kT}} + \frac{q\phi_s}{kT} - 1\right) + \frac{n_0}{p_0}\left(e^{\frac{q\phi_s}{kT}} - \frac{q\phi_s}{kT} - 1\right)\right]^{\frac{1}{2}}$$

Where, we have introduced a new term, the Debye screening length,

$$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 p_0}}$$

- The Debye length is a very important concept in semiconductors. It gives us an idea of the distance scale in which charge imbalances are screened or smeared out .
- By using Gauss's law at the surface, we can relate the integrated space charge per unit area to the electric displacement, keeping in mind that the electric field or displacement deep in the substrate is zero.

$$Q_s = -\epsilon_s \mathcal{E}_s$$

- The space charge density per unit area is plotted as a function of the surface potential ϕ_s in Fig. 1.31
- When the surface potential is zero **(flat band conditions)**, the net space charge is zero. This is because the fixed dopant charges are cancelled by the mobile carrier charges at flat band.

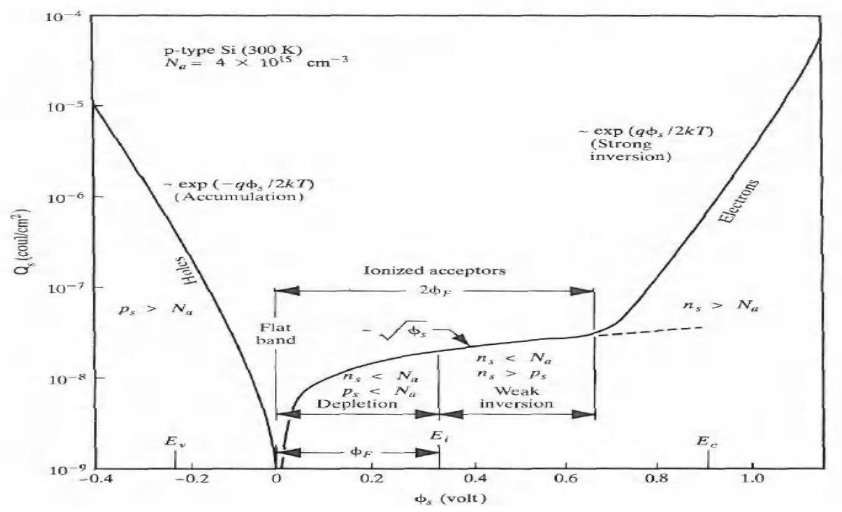


Fig. 1.31: Variation of space-charge density in the semiconductor as a function of the surface potential (J>5 for p-type silicon with *Na* = 4 X 1015 cm-3 at room temperature. p5and *ns* are the hole and electron concentrations at the surface, *$F* is the potential difference between the Fermi level and the intrinsic level of the bulk.

- When the surface potential is negative, it attracts and forms an accumulation layer of the majority carrier holes at the surface. Hence, the space charge for small positive surface potentials increases as ~ ϕs

- The depletion width typically extends over several hundred nm. At some point, the band-bending is twice the Fermi potential ϕF , which is enough for the onset of strong inversion.
- The charge distribution, electric field, and electrostatic potential for the inverted surface are sketched in Fig. 1.32.
- In this approximation the charge per unit area due to uncompensated acceptors in the depletion region is -qNaW. The positive charge Q_m on the metal is balanced by the negative charge Qs in the semiconductor, which is the depletion layer charge plus the charge due to the inversion region Qn :

  Qm = -Qs = qNaW - Qn
- Actually, the width of this region is generally less than 100 Ao. Thus we have neglected it in sketching the electric field and potential distribution. In the potential distribution diagram we see that an applied voltage V appears partially across the insulator {Vt) and partially across the depletion region of the semiconductor ϕs :

V=Vi +ϕs

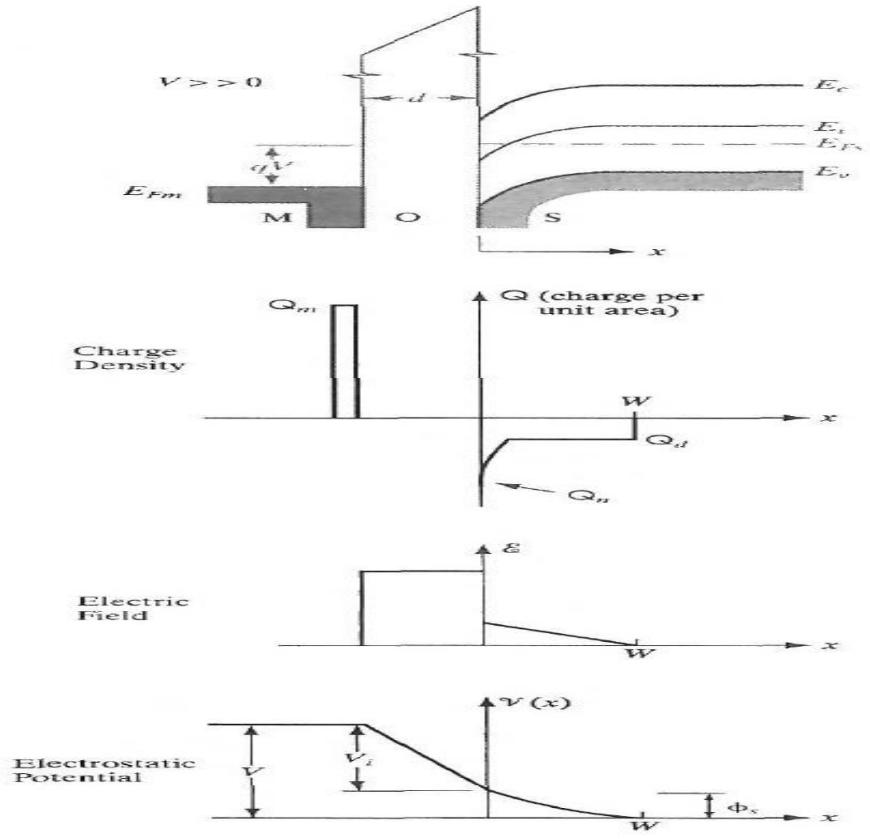


Fig. 1.3.2: Approximate distributions of charge, electric field, and electrostatic potential in the ideal MOS capacitor in inversion. The relative width of the inverted region is exaggerated for illustrative purposes, but is neglected in the field and potential diagrams.

- The voltage across the insulator is obviously related to the charge on either side, divided by the capacitance:

  $$Vi = -Qsd / \epsilon i = -Qs / Ci$$

  Where, ϵi is permittivity of the insulator and C, is the insulator capacitance per unit area. The charge Qs will be negative for the n channel, giving a positive Vt.
- For an n+-p junction the depletion region extends almost entirely into the p region:

  $$W = \left[\frac{2\epsilon_s \phi_s}{qN_a}\right]^{1/2}$$

- This depletion region grows with increased voltage across the capacitor until strong inversion is reached. After that, further increases in voltage result in stronger inversion rather than in more depletion. Thus the maximum value of the depletion width is

  $$W_m = \left[\frac{2\epsilon_s \phi_s(\text{inv.})}{qN_a}\right]^{1/2} = 2\left[\frac{\epsilon_s kT \ln(N_a/n_i)}{q^2 N_a}\right]^{1/2}$$

- We know the quantities in this expression, so Wm can be calculated. The charge per unit area in the depletion region Qdat strong inversion is

  $$Q_d = -qN_a W_m = -2(\epsilon_s q N_a \phi_F)^{1/2}$$

- The applied voltage must be large enough to create this depletion charge plus the surface potential ϕs(inv.).The threshold voltage required for strong inversion, is

  $$V_T = -\frac{Q_d}{C_i} + 2\phi_F \quad (ideal\ case)$$

- This assumes the negative charge at the semiconductor surface Qs at inversion is mostly due to the depletion charge Q_d. The threshold voltage represents the minimum voltage required to achieve strong inversion.

1.9 The Capacitance-Voltage characteristics of this ideal MOS structure :

- The capacitance-voltage characteristics of this ideal MOS structure Fig. 3.22 vary depending on whether the semiconductor surface is in accumulation, depletion, or inversion.

- Since the capacitance for MOSFETs is voltage dependent, we must use the more general expression for the voltage-dependent semiconductor capacitance

$$C_s = \frac{dQ}{dV} = \frac{dQ_s}{d\phi_s}$$

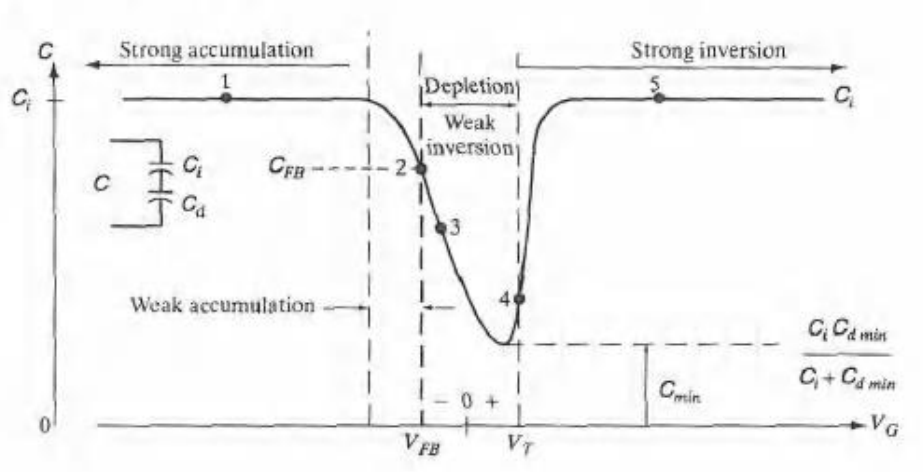


Fig. 1.33: The dashed curve for *V*>Vr is observed at high measurement frequencies. The flat band voltage V_{FB},when the semiconductor is in depletion, the semiconductor capacitance *Cs* is denoted as *Cj*.

- Actually, if one looks at the electrical equivalent circuit of a MOS capacitor or MOSFET, it is the series combination of a fixed, voltage-independent gate oxide (insulator) capacitance, and a voltage-dependent semiconductor capacitance, such that the overall MOS capacitance becomes voltage dependent. The semiconductor capacitance itself can be determined from the slope of the Qs versus ϕs plot (above Fig).Change of each stage of characteristics arerepresented as a points in the figure 1.33.
- **Point 1:** It is clear that the semiconductor capacitance in accumulation is very high (the slope is so steep;) i.e., the accumulation charge changes a lot with surface potential. Hence, the series capacitance in accumulation is basically the insulator capacitance, C_i. Since, for negative voltage, holes are accumulated at the surface, the MOS structure appears almost like a parallel-plate capacitor, dominated by the insulator properties $C_i = \epsilon_i/d$ (point 1 in Fig. 1.33).

- Point 2: As the voltage becomes less negative, the semiconductor surface is depleted. Thus a depletion-layer capacitance Cd is added in series with Ci .

$$Ci = \epsilon s / W$$

Where, ϵs is the semiconductor permittivity and

W is the width of the depletion layer.

- The total capacitance is

$$C = \frac{C_i C_d}{C_i + C_d}$$

- The capacitance decreases as W grows from flat band (point 2)
- **Point 3 & 4:**Past weak inversion (point 3), until finally strong inversion is reached at VT (point 4). In the depletion region, the small signal semiconductor capacitance depends on the variation of the (depletion) space charge with surface potential. Since the charge increases as ~(ϕs)1/2 the depletion capacitance will obviously decrease as 1/(ϕs)1/2, exactly as for the depletion capacitance of a p-n junction.
- **Point 5:**After inversion is reached, the small signal capacitance depends on whether the measurements are made at high (typically ~1 MHz) or low (typically -1-100 Hz) frequency, where "high" and "low" are with respect to the generation-recombination rate of the minority carriers in the inversion layer.
- If the gate bias is changed slowly, there is time for minority carriers to be generated in the bulk, drift across the depletion region to the inversion layer, or go back to the substrate and recombine. We can observe that the inversion charge increases exponentially with ϕ_s. Hence, the low frequency MOS series capacitance in strong inversion is basically C_i once again (point 5).

1.9.1 The frequency dependence of the capacitance in accumulation

- We get a very high capacitance both at low and high frequencies because the majority carriers in the accumulation layer can respond much faster than minority carriers. While minority carriers respond on the time scale of generation-recombination times (typically hundreds of microseconds in Si), majority carriers respond on the time scale of the dielectric relaxation time, $\tau_D = \rho\epsilon$, where, ρ is the resistivity and ϵ is the permittivity.

- As an interesting aside, it may be pointed out that in inversion, although the high-frequency capacitance for MOS capacitors is low, it is high (= C_i) for MOSFETs because now the inversion charge can flow in readily and very fast (τ_D) from the source/drain regions rather than having to be created by generation-recombination in the bulk.

1.10 Special diodes

1.10.1 The Schottky-barrier diode

- These diodes are designed to have a very fast switching time which makes them a great diode for digital circuit applications. They are very common in computers because of their ability to be switched on and off so quickly.

Fig. 1.34 Circuit symbol of photodiode

- **Operation:** The forward voltage drop (V), reverse-recovery time (t), and junction capacitance (C) of Schottky diodes are closer to ideal than the average "rectifying" diode. This makes them well suited for high frequency applications. Unfortunately, though, Schottky diodes typically have lower forward current (I) and reverse voltage (V and V) ratings than rectifying diodes and are thus unsuitable for applications involving substantial amounts of power. Though they are used in low voltage switching regulator power supplies. Schottky diode technology finds broad application in high-speed computer circuits, where the fast switching time equates to high speed capability, and the low forward voltage drop equates to less power dissipation when conducting.
- **Advantages**
  - Schottky diodes have a shorter reverse recovery time.
  - High frequency
  - Low forward voltage drop
  - Low heat dissipation
  - Low loss

- Low turn on voltage
- Fast recovery time
- Low junction capacitance

➢ **Disadvantages**

- Cost and size.

➢ **Applications**

- The Schottky barrier diodes are widely used in the electronics industry finding many uses as diode rectifier. Its unique properties enable it to be used in a number of applications where other diodes would not be able to provide the same level of performance. In particular it is used in areas:
- *RF mixer and detector diode*: The Schottky diode has come into its own for radio frequency applications because of its high switching speed and high frequency capability. In view of this Schottky barrier diodes are used in many high performance diode ring mixers. In addition to this their low turn-on voltage and high frequency capability and low capacitance make them ideal as RF detectors.
- *Power rectifier:* Schottky barrier diodes are also used in high power applications, as rectifiers. Their high current density and low forward voltage drop mean that less power is wasted than if ordinary PN junction diodes were used. This increase in efficiency means that less heat has to be dissipated, and smaller heat sinks may be able to be incorporated in the design.

1.10.2 Varactors

➢ Varactor diode is basically a reverse biased PN junction, which utilizes the capacitance of depletion layer. It is also known as varicap, voltcap or tuning diode. It is used as voltage variable capacitor.

➢ When the reverse bias voltage increases, the depletion region widens. This increases the dielectric thickness, which in turn reduces the capacitance.

$$C_T = A\varepsilon/w \quad \Rightarrow C_T \alpha\ 1/w \Rightarrow \text{as 'w' increases, } C_T \text{ decreases}$$

➢ When the reverse bias voltage decreases, the depletion layer narrows down. This decreases the dielectric thickness, which in turn increases the capacitance. The depletion layer acts as insulator preventing conduction between the N and P regions of the diode, just like a dielectric, which separates the two plates of the capacitor.

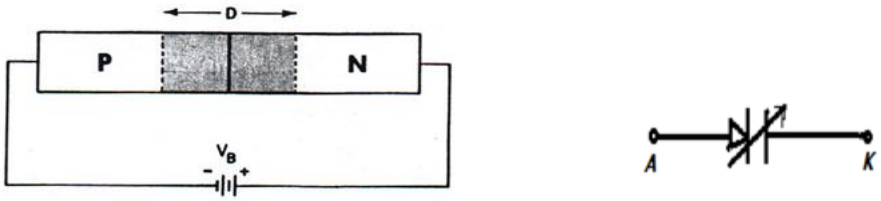


Fig. 1.35 Varactor diode construction and its symbol

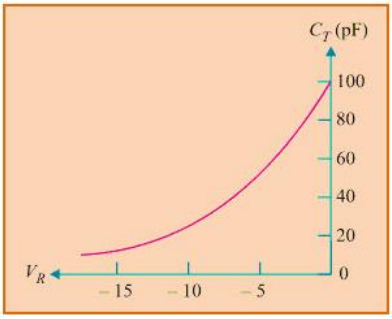


Fig. 1.36 Varactor diode characteristics

- **Applications**
  - used in FM radio receivers
  - used in TV Receivers

1.10.3 Photodiodes

- Photodiode is a light sensitive device, also called photo detector, which converts light signals into electrical signals.

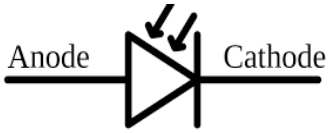


Fig. 1.37 Circuit symbol of photodiode

- The diode is made of a semiconductor PN junction kept in a sealed plastic or glass casing. The cover is so designed that the light rays are fall on one surface across the junction.
- When light falls on reverse biased PN photodiode junction, electron-hole pairs are created.

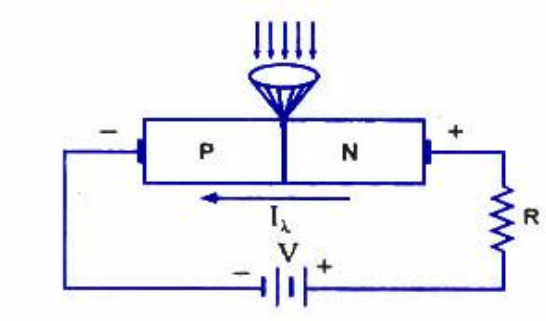


Fig. 1.38 Basic biasing arrangement and construction of photodiode

- The movement of these electron-hole pairs in a properly connected circuit results in current flow.
- The magnitude of photocurrent depends on the number of charge carriers generated. This current is also affected by the frequency of the light falling on the junction of photodiode.
- The magnitude of the current under large reverse bias is given by

$$I = I_o[\exp(V / \eta V_T) - 1]$$

Where, I_o is reverse saturation current or dark current, η =1 for Ge and 2 for Si.

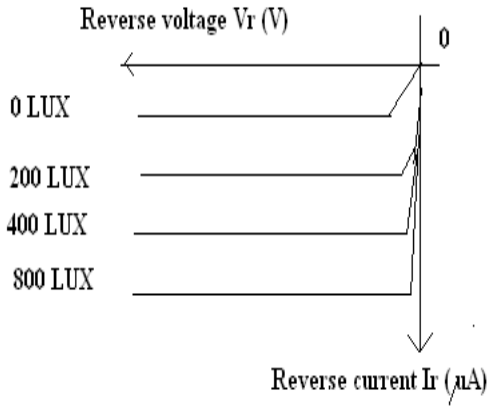


Fig. 1.39 Photo Diode characteristics

- **Advantages**
  - Low resistance
  - Very good spectral response
  - Fastest photo detector
- **Disadvantages**
  - Light sensitive device
  - Dark current increased with temperature

- Should not exceed the working temperature limit specified by the manufactures.

➢ **Applications:**

- Light detector
- Demodulators
- Encoders
- Optical Communication System
- High speed counting and switching circuits

1.10.4 Light-Emitting Diodes (LEDs)

➢ A PN junction diode, which emits light when forward biased, is known as Light Emitting Diode (LED).The amount of light output is directly proportional to the forward current

➢ The circuit symbol of LED is shown in figure

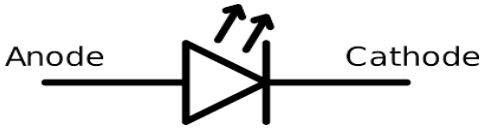


Fig. 1.40 Circuit symbol of Light Emitting Diode

➢ A P-type layer is grown on the N-type layer. When an external positive voltage is applied to the P- type region with respect to N- type, both the depletion region width and the resulting potential barrier are reduced and the diode is said to be forward biased.

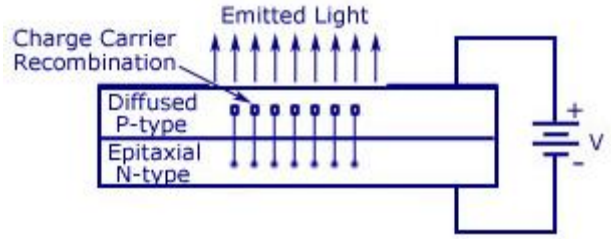


Fig. 1.41 Constructional diagram of LED

➢ When LED is forward biased, the electrons and holes moves towards the junction and recombination takes place.

➢ After recombination, the electrons lye in the conduction band of N- region, holes lye in the valence band of P-region.

➢ The difference of energy between the conduction band and valence band is radiated in the form of light energy.

$$E_g = hf = hc/\lambda$$

$$\Rightarrow \lambda = 1.24/E_g$$

Where, λ= wave length of light

h=Plank's constant $=6.626*10^{-34}$Jsec

c= Velocity of light$=3*10^{8}$ m/sec

- **Materials used:** GaAs (Infrared light(invisible)), GaAsP (red or yellow visible light), GaP (red or green visible light)
- **Advantages**
  - Very low voltage and current are enough to drive the LED.
  - Voltage range – 1 to 2 volts.
  - Current – 5 to 20mA.
  - Total power output will be less than 150 mW
  - The response time is very less – only about 10 nanoseconds.
  - The device does not need any heating and warm up time.
  - Miniature in size and hence light weight.
  - Have a rugged construction and hence can withstand shock and vibrations.
  - An LED has a life span of more than 20 years.
- **Disadvantages**
  - A slight excess in voltage or current can damage the device.
  - The device is known to have a much wider bandwidth compared to the laser.
  - The temperature depends on the radiant output power and wavelength.
- **Applications**

  LEDs are used in a wide variety of applications. Some typical applications of LEDs include:
  - On-off indicator
  - Traffic lights
  - Visual displays
  - Medical applications
  - Signs and indicators
  - in remote controls
  - in optical communications as Opto-couplers and opto-isolators

Assignment-Cum-Tutorial Questions

A. Questions testing the remembering / understanding level of students

I) Objective Questions

1. To double the hole current in $P^+ - N$ junction..... [ ]
   a) Double the P^+ doping
   b) Double the N doping
   c) Reduce the N doping by a factor of two.
   d) Reduce the P doping by a factor of two.
2. What is meant by Zener breakdown?
3. What is meant by Avalanche breakdown? (or) What is the effect of Impact Ionization in lightly doped diodes?
4. What is Schottky effect?
5. List the applications of metal-semiconductor junctions.
6. Sketch the I-V characteristics of an ideal diode.
7. For a decade change in current, the diode voltage changes by.....(from diode I-V equation)
8. Sketch the C-V characteristics of an ideal MOS capacitor
9. A diode for which you can change the reverse bias, and thus vary the capacitance is called as..... [ ]

   a) Tunnel diode b) Varactor diode

   b) c) Zener diode d) Switching diode

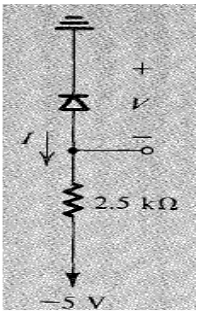
10. What is the difference between LED and photo diode?
11. Find the correct match between Group 1 and Group 2 :

Group 1	**Group 2**
a) Varactor Diode	1) Voltage reference
b) PIN diode	2)High frequency switch
c)Zener diode	3) Tuned circuits
d)Schottky diode	4)Current controlled attenuator

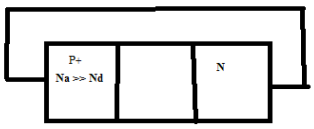
12. Match items in Group 1 with items in Group 2, most suitably.

Group 1	**Group 2**
a. LED	1.heavy doping
b. Avalanche photo diode	2. Coherent radiation
c. Tunnel diode	3.Spontaneousemission.
d. LASER	4.Current gain

13. Assuming the diodes to be ideal, find the values of I and V in the circuits shown.

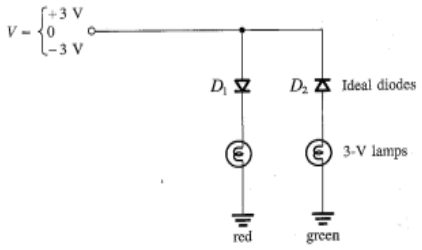


14. In a uniformly doped abrupt p-n junction the doping level of n-side is four times the doping level of the p-side. What is the ratio of depletion width of n-side vs. p-side?
15. A p^+-n junction has built-in potential of 0.8V. The depletion layer width at a reverse bias of 1.2V is 2μm. For a reverse bias of 7.2V, the depletion layer width will be.....
16. Consider an abrupt p-n junction at T=300^{o}K shown in fig. The depletion region width X_n of the N-side of the junction is 0.2μm and the permittivity of Si(ϵ_{si}) is 1.044x10 $^{-12}$F/m, $N_d 10^{16}/cm^3$. At the junction the approximate value of the electric field (in kV/cm) is.....

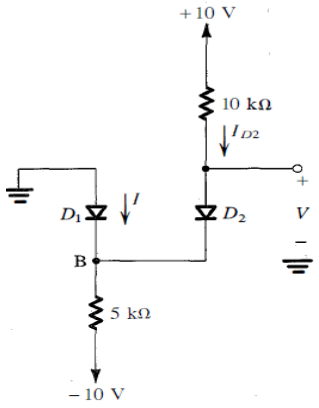


17. The circuit shown can be used in a signaling system using one wire plus a common ground return. At any moment, the input has one of

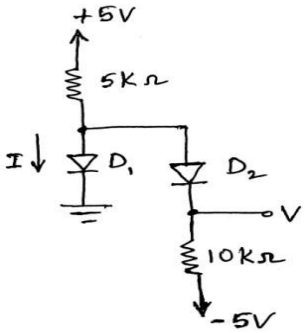
three values: +3V, 0V, -3V. What is the status of the lamps for each input value?



18. Assuming the diodes to be ideal, find the values of I and V in the circuits shown.

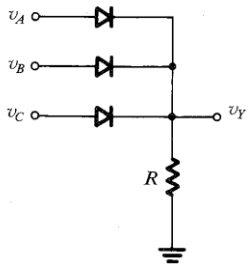


19. Compute the values of I and V in the figure (Diodes used are ideal).



20. For the logic gate shown in figure, assume ideal diodes and input voltage levels of 0V and +5V. Find a suitable value for R so that the

current required from each of the input signal sources does not exceed 0.1mA.



21. The static characteristics of an adequately forward biased p-n junction is a straight line, if the plot is _____ [ ]

a) log I vs log V b) log I vs V c) I vs log V d) I vs V

22. In a P^+-N junction under reverse bias, the magnitude of electric field is maximum at ____ [ ]

a) the edge of depletion region on P-side

b) the edge of depletion region on N-side

c) the P^+-N junction

d) the centre of depletion region on N-side

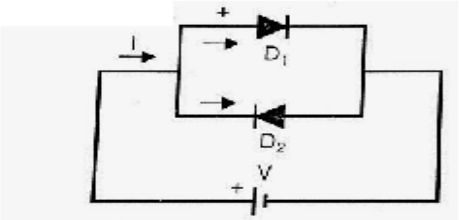
23. In a p+-n junction, the n-doping N_d is doubled. **How** do the following change if everything else remains unchanged? Indicate only increase or decrease.

(a) Junction capacitance
(b) Built-in potential
(c) Breakdown voltage
(d) Ohmic losses

24. Illustrate the effects of forward bias and reverse bias at junction for the following parameters:

a) depletion region width
b) electrostatic potential
c) energy band diagram
d) particle flow and current directions

25. In the circuit shown below, the current voltage relationship when D_1 and D_2 are identical Germanium diodes is given by _____ [ ]



(A) $V = \frac{KT}{q}\sinh\left(\frac{I}{2}\right)$ (B) $V = \frac{KT}{q}ln\left(\frac{I}{I_o}\right)$

(C) $V = \frac{KT}{q}\sinh^{-1}\left(\frac{I}{2}\right)$ (D) $V = \frac{KT}{q}[Exp(-I) - 1]$

II) Descriptive Questions

1. Explain the properties of an equilibrium p-n junction with neat sketches.
2. Sketch and explain the variation of charge density, electric field, and electrostatic potential within the transition region of a p^+-n junction.

   or

   Justify the qualitative argument that a deep penetration is necessary in lightly doped material to "uncover" the same amount of space charge as for a short penetration into heavily doped material.
3. With neat sketches give the qualitative description of current flow at junction and derive the diode current equation which describes the total current through the diode for either forward or reverse bias.
4. Explain the breakdown mechanisms of a p-n junction under reverse bias condition.
5. Sketch and explain the terminal characteristics of a diode and how temperature effects these characteristics.

   or

   Explain the operation of a diode in forward and reverse bias region using V-I characteristics .

6. What is the effect of forward and reverse bias on rectifying contacts(with neat sketches.) and explain how it is different with the ohmic contacts?
7. Draw and explain the capacitance-voltage characteristics of a MOS capacitor.
8. Brief out the following:
    a. Varactor diode.
    b. Schottky barrier diode.
    c. Photo diode.
    d. LED

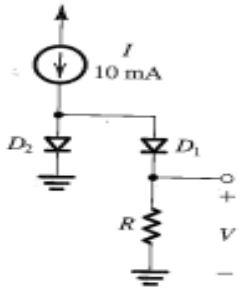
II) Descriptive Questions

1. An abrupt Si p-n junction has $N_a = 10^{17}$ cm^{-3} on the p side and $N_d = 10^{16}$ cm^{-3} on the n side. At 300^o K, (a) calculate the Fermi levels, draw an equilibrium band diagram, and find V_0 from the diagram; (b) compare the result from (a) with V_o calculated using expression.
2. A p^+-n junction has $N_a=10^{20}$cm^{-3}, $N_d=10^{17}$cm^{-3}. What is it's
    a) built in potential b)W_{dep} C) X_{no} d) X_{po}
3. A Si p-n junction with cross-sectional area A = 0.001 cm^2 is formed with $N_a = 10^{15}$cm^{-3}, $N_d = 10^{17}$ cm^{-3}. Calculate:
    (a) Contact potential, V_0.
    (b) Space-charge width at equilibrium (zero bias).
    (c) Current with a forward bias of 0.5V. Assume μ_n = 1500 cm^2/V-s, μ_p = 450 cm^2/V-s, $\tau_n = \tau_p$ = 2.5 ms. Which of the carries contributes most of the current and why? If you want to double the electron current, what should you do?
4. An abrupt p^+-n junction is formed in Si with a donor doping of $N_d = 10^{15}$ cm^{-3}. What is the minimum thickness of the n region that will ensure avalanche breakdown rather than punch-through?

5. Listed below are the results of measurements taken on several different junction diodes. For eaqch diode, the data provided are the diode current I, the corresponding diode voltage V, and the diode voltage at a current I/10. In each case, estimate Is, n, and the diode voltage at 10I.

   (a) 10mA, 700mV, 600mV (b) 1mA, 700mV, 600mV

6. For the circuit shown, both diodes are identical, conducting 10mA at 0.7 V and 100 mA at 0.8 V. Find the value of R for which V = 80 mV.



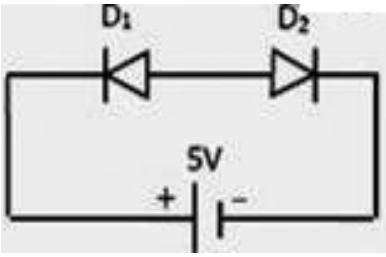
7. A one-sided abrupt Si N^+ - P junction has an area of 10^{-4} cm^2. If N_d is very high, $N_a = 10^{23}$ m^{-3}, ϵ_{si} =11.8, reverse voltage =100V, T=300^o K, find the peak electric field at the junction.
8. In a one-sided abrupt Si n^+-p junction (area = 0.0001 cm^2), we have the following parameters at 300 K:

n-side	**p-side**
N_d=very high	$N_a=10^{17}cm^{-3}$
τ_p=10μs	τ_n= 1us
μ_n=100cm^2/V-s	μ_p=700 cm^2/V-s
μ_p=450 cm^2/V-s	μ_n=200cm^2/V-s

Calculate the peak electric field at the junction and the depletion capacitance at a reverse bias of 100 V. (Hint: This is much higher than the contact potential, and remember that this is a one-sided junction!) For a certain forward bias, we have a current flow of 20 mA in this device. Calculate the total excess stored electron charge on the

p side for this bias and the electric field far from the depletion region on the p side.

9. Two identical silicon junction diodes, D_1 and D_2 are connected back to back as shown. The reverse saturation current I_S of each diode is 10^{-8} Amps and the breakdown voltage is 50 volts. Evaluate the voltage V_{D1} and V_{D2} across the diode D_1 and D_2 by assuming KT/q to be 25mV.

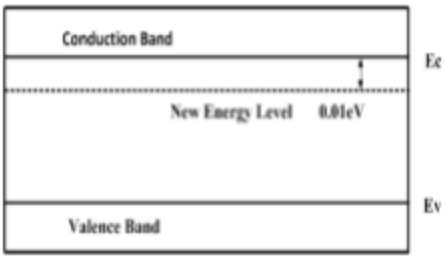


10. In a uniformly doped abrupt P – N junction the doping level of the n – side is four times the doping level of the p – side the ratio of the depletion layer width of n – side verses p – side is _____

    In an abrupt P – N junction, the doping concentrations on the P – side and N – side are $9 \times 10^{16}/cm^3$ *and* $1 \times 10^6\ /cm^3$ respectively. The P – N junction is reverse biased and the total depletion width is 3 μm. Determine depletion width on the P side ?

D. GATE previous questions

1. A small percentage of impurity is added to an intrinsic semiconductor at 300 K. Which one of the following statements is true for the energy band diagram shown in the following figure? (GATE 2016) [ ]



(A) Intrinsic semiconductor doped with pentavalent atoms to form n-type semiconductor

(B) Intrinsic semiconductor doped with trivalent atoms to form n-type semiconductor

(C) Intrinsic semiconductor doped with pentavalent atoms to form p-type semiconductor

(D) Intrinsic semiconductor doped with trivalent atoms to form p-type semiconductor

2. Consider a silicon p-n junction with a uniform acceptor doping concentration of 10^{17} cm^{-3} on the p- side and a uniform donor doping concentration of 10^{16} cm^{-3}on the n-side. No external voltage is applied to the diode. Given: kT /q =26mV, n_i= 1.5* 10^{10} cm^{-3} , ε_{si}= $12\varepsilon_o$,ε_o= 8.85* 10^{-14} F/ m, and q=1.6*10^{-19}C .The charge per unit junction area (nC cm^{-2}) in the depletion region on the p-side is ..... (GATE 2016)

3. Consider avalanche breakdown in a silicon p^+ n junction. The n-region is uniformly doped with a donor density ND. Assume that breakdown occurs when the magnitude of the electric field at any point in the device becomes equal to the critical field E crit. Assume Ecrit to be independent of N_D. If the built-in voltage of the p^+ n junction is much smaller than the breakdown voltage, V_{BR}, the relationship between VBR and N_D is given by (GATE 2016)

[ ]

(A) $V_{BR} \times \sqrt{N_D}$ = constant

(B) $\sqrt{V_{BR}} \times N_D$ = constant

(C) $V_{BR} \times N_D$ = constant

(D) N_D/V_{BR} = constant

4. The ratio of the mobility to the diffusion coefficient in a semiconductor has the units [ ] (GATE 2009)

(A) V^{-1} (B) $cm.V^{-1}$ (C) $V.cm^{-1}$ (D) V .s

5. Which of the following is NOT associated with a p n - junction ? [ ] (GATE 2008)

   (A) Junction Capacitance (B) Charge Storage Capacitance

   (C) Depletion Capacitance (D) Channel Length Modulations

6. Which of the following is true? [ ] (GATE 2008)

   (A) A silicon wafer heavily doped with boron is a p+ substrate

   (B) A silicon wafer lightly doped with boron is a p+ substrate

   (C) A silicon wafer heavily doped with arsenic is a p+ substrate

   (D) A silicon wafer lightly doped with arsenic is a p+ substrate

7. Consider the following assertions. (GATE 2008) [ ]

   S1 : For Zener effect to occur, a very abrupt junction is required.

   S2 : For quantum tunneling to occur, a very narrow energy barrier is required.

   Which of the following is correct ?

   (A) Only S2 is true

   (B) S1 and S2 are both true but S2 is not a reason for S1

   (C) S1 and S2 and are both true but S2 is not a reason for S1

   (D) Both S1 and S2 are false

8. In a p n^+ junction diode under reverse biased condition the magnitude of electric field is maximum at [ ] (GATE 2007)

   (A) the edge of the depletion region on the p-side

   (B) the edge of the depletion region on the n-side

   (C) the p n+ junction

   (D) the centre of the depletion region on the n-side

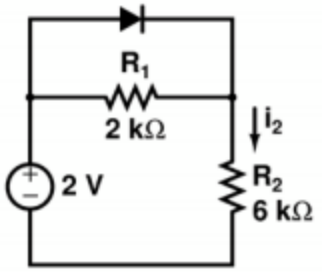
9. A p n^+ junction has a built-in potential of 0.8 V. The depletion layer width a reverse bias of 1.2 V is 2 mm. For a reverse bias of 7.2 V, the depletion layer width will be [ ] (GATE 2007)

(A) 4 mm (B) 4.9 mm (C) 8 mm

(D) 12 mm

(D) no relationship among these band gaps exists

10. Assume that the diode in the figure has V_{on}= 0.7V, on but is otherwise ideal. The magnitude of the current i_2 (in mA) is equal to _____. (GATE 2016)



11. In a forward biased pn junction diode, the sequence of events that best describes the mechanism of current flow is (GATE 2013) [ ]

(A) injection, and subsequent diffusion and recombination of minority carriers

(B) injection, and subsequent drift and generation of minority carriers

(C) extraction, and subsequent diffusion and generation of minority carriers

(D) extraction, and subsequent drift and recombination of minority carriers

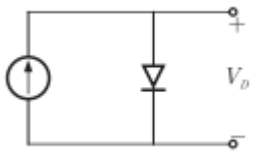
12. A silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10°C, the forward bias voltage across the PN junction [ ] (GATE 2011)

(A) increases by 60 mV (B) decreases by 60 mV

(C) increases by 25 mV (D) decreases by 25 mV

13. In the figure, silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20cC V, D is found to be 700 mV. If

the temperature rises to 40cC V, D becomes approximately equal to…… (GATE 2008)



(A) 740 mV (B) 660 mV (C) 680 mV (D) 700 mV

14. In a MOS capacitor with an oxide layer thickness of 10 nm, the maximum depletion layer thickness is 100 nm. The permittivities of the semiconductor and the oxide layer are ϵ_S and ϵ_{ox} respectively. Assuming $\epsilon_S / \epsilon_{ox} = 3$, find the ratio of the maximum capacitance to the minimum capacitance of this MOS capacitor. (GATE 2015)

Unit – II

Objectives:

- To introduce the Modelling concepts of pn junction diode, zener diode and their applications

Syllabus: Modelling the diode forward characteristic, Zener diode model, use of the Zener as a shunt regulator, temperature effects, design of Zener voltage regulator, the SPICE models for junction and Zener diodes, Diode logic gates, diode as a rectifier, design of power supply using bridge rectifier; limiting and clamping circuits.

Outcomes:

At the end of the unit, student will be able to

- Understand the models for pn junction and Zener diodes
- Understand the applications of Zener diode as regulator
- Understand the applications of junction diode as rectifiers and logic gates
- Understand the applications of junction diode as limiting and clamping circuits

DIODE MODELS AND APPLICATIONS

2.1 Modeling the diode forward characteristics

- To model the diode forward characteristic, we need to analyse the circuit employing forward conducting diodes as shown in Fig. 2.1. It consists of a dc source V_{DD}, a resistor R and a diode.

i) The exponential model: The most accurate description of the diode operation in the forward region is provided by the exponential model.

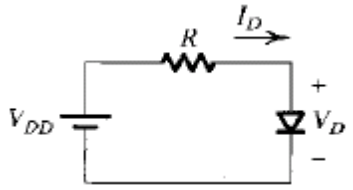


Fig. 2.1: A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting

- Assume V_{DD} is greater than 0.5 V, so the diode current will be much greater than I_S, we can represent the diode i-v characteristic by the exponential relationship

$$I_D = I_S e^{V_D/\eta V_T} \quad \text{----------} \quad (2.1.1)$$

- Other equation that governs circuit operation is obtained by writing KVL equation,

$$I_D = (V_{DD} - V_D)/R \quad \text{----------} \quad (21.2)$$

- Assuming that the two parameters I_S and η are known, equations (2.1.1) and (2.1.2) are two equations in the two unknown quantities I_D and V_D. Two alternate ways for obtaining the solution are graphical and iterative analysis.

ii) Graphical analysis using the Exponential model

- Graphical analysis is performed by plotting equations (2.1.1) and (2.1.2) on the *i-v* plane

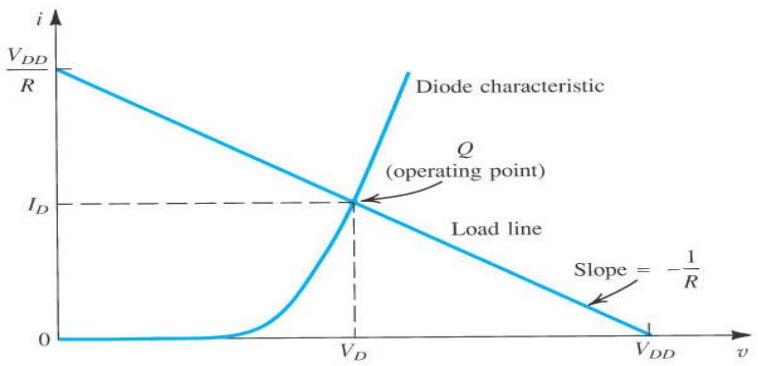


Fig. 2.2: Graphical analysis of the circuit in fig.2.1 using the exponential diode model.

- The solution can then be obtained as the coordinates of the point of intersection of the two graphs as shown in Fig. 2.2.
- The curve represents the exponential diode equation and the straight line represents the equation (2.1.2). Such a straight line is called load line.
- The load line intersects the diode curve at point Q, which represents the operating point of the circuit. Its coordinates gives the values of I_D and V_D.

iii) Iterative analysis using the Exponential model

- Equations (2.1.1) and (2.1.2) can be solved using a simple iterative procedure as shown in the example given below:
- **Eg:** Determine the current I_D and the diode voltage V_D for the circuit shown in Fig. 2.1 with V_{DD} = 5 V and R = 1 KΩ. Assume that the diode has a current of 1 mA at a voltage of 0.7 V and that its voltage drop changes by 0.1 V for every decade change in current.

Solution:

To begin the iteration, we assume that V_D = 0.7 V and use Eq. (2.1.2) to determine the current, $I_D = (V_{DD} - V_D)/R = (5\text{-}0.7)/1 = 4.3$ mA

Using the equation $V_2 - V_1 = 2.3\eta V_T \log (I_2/I_1)$

For our case, $2.3\eta V_T = 0.1$ V. Thus, $V_2 = V_1 + (0.1)1\log (I_2/I_1)$

Substituting V_1 = 0.7 V, I_1 = 1 mA, and I_2 = 4.3 mA results in V_2 = 0.763 V.

Thus the results of the first iteration are I_D = 4.3 mA and V_D = 0.763 V.

The second iteration proceeds in a similar manner:

$$I_D = (5 - 0.63) / 1\ K\Omega = 4.237\ mA$$

$$V_2 = 0.63 + 0.1 \log (4.237/4.3) = 0.762\ V$$

Thus the second iteration yields I_D = 4.237 mA and V_D = 0.762 V. Since these values are not much different from the values obtained after the first iteration, no further iterations are necessary, and the solution is I_D = 4.237 mA and V_D = 0.762 V.

iv) The need for rapid analysis

- The iterative analysis procedure is simple and yields accurate results after two or three iterations. There are situations in which the effort and time required are greater to justify the result. Hence rapid analysis is necessary.
- Through quick analysis, the designer is able to evaluate various possibilities before deciding on a suitable circuit design. To speed up the analysis process one must be content with less precise results.
- Accurate analysis of almost final design can be obtained with the use of computer circuit-analysis program such as SPICE. The results of such an analysis can then be used to fine-tune the design.

v) The Piecewise-Linear model

- In this model, the exponential curve is approximated by two straight lines, line A with zero slope and line B with a slope of $1/r_D$.

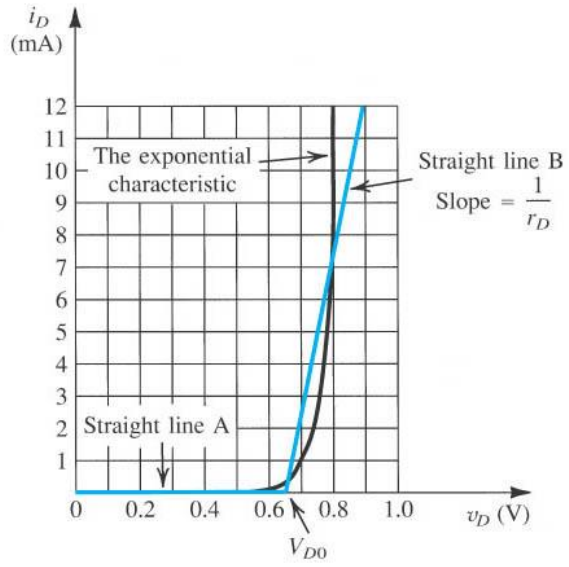


Fig. 2.3: Approximating the diode forward characteristic with two straight lines: the piecewise-linear model

- Over the current range of 0.1 mA to 10 mA, the voltages predicted by the straight line

model shown differ from those predicted by the exponential model by less than 50 mV.

- The straight lines of piecewise-linear model shown in Fig. 2.3 can be described by

$$i_D = 0, \; v_D \le V_{D0}$$

$$i_D = (v_D - V_{D0}) / r_D, \quad v_D \ge V_{D0} \quad \text{---------- (2.1.3)}$$

where, V_{D0} is the intercept of line B on the voltage axis and r_D is the inverse of the slope of line B.

- The piecewise-linear model described by equation (2.1.3) can be represented by the equivalent circuit shown in Fig. 2.4. An ideal diode included in this model is to constrain i_D to flow in the forward direction only. This model is also known as the **battery – plus – resistance** model.

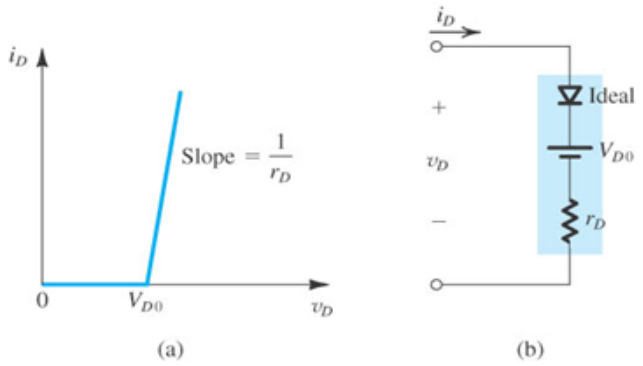


Fig. 2.4: Piecewise-linear model of the diode forward characteristic and its equivalent circuit representation

vi) The Constant-Voltage-Drop model

- It can be obtained by if we use a vertical straight line to approximate the fast-rising part of the exponential curve. The resulting model says that a forward-conducting diode exhibits a constant-voltage-drop V_D which is 0.7 V.
- This model predicts the diode voltage to within ±0.1 V over the current range of 0.1 mA to 10 mA. The constant-voltage-drop model can be represented by the equivalent circuit as shown in Fig. 2.5.
- If we assume this model while analyzing the diode circuits, we get

For $i_D > 0$: $\quad V_D = 0.7V$,

$v_D = 0.7$ V $\quad I_D = (V_{DD} - 0.7) / R$

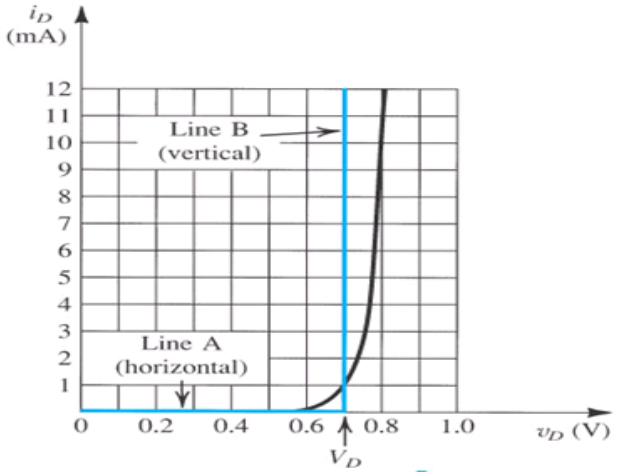


Fig. 2.5: Development of constant-voltage-drop model of the diode forward characteristics. A vertical straight line B is used to approximate the fast-rising exponential.

vii) The Ideal-Diode model

- If we neglect the diode voltage drop while calculating the diode current, it results the Ideal-diode model. i.e.,

$$\text{For } i_D > 0;$$
$$v_D = 0$$

- This model can be used in determining which diodes are ON and which are OFF in a multi diode circuit. The ideal diode model of diode forward characteristic and its equivalent circuit representation are shown in Fig. 2.6.

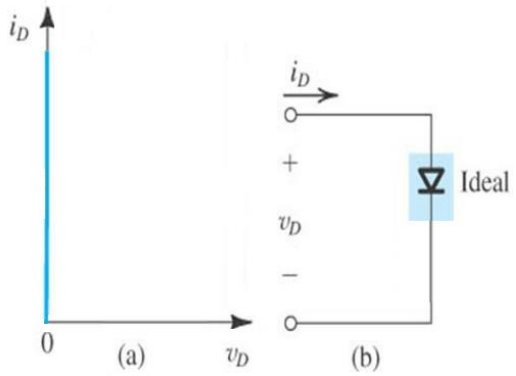


Fig. 2.6: The ideal diode model of the diode forward characteristics and its equivalent circuit representation.

viii) The small-signal model

- There are applications in which a diode is biased to operate at a point on the forward i-v

characteristic and a small ac signal is superimposed on the dc quantities. For this, we need to determine the dc operating point (V_D and I_D) of the diode using any one of the models. Most frequently, constant-voltage-drop model is utilized.

- For small-signal operation around the dc bias point,
  - The diode is to be modeled by a resistance equal to inverse of the slope of tangent to the *i-v* characteristic at the bias point.
  - Concept of biasing a nonlinear device is to restrict signal excursion to almost linear segment of its characteristic around the bias point.
- Consider the circuit shown in Fig. 2.7 (a) and the corresponding graphical representation in Fig. 2.7 (b). A dc voltage V_D represented by a battery, is applied to the diode and a time-varying signal $v_d(t)$, assumed to have triangular waveform, is superimposed on the dc voltage V_D.

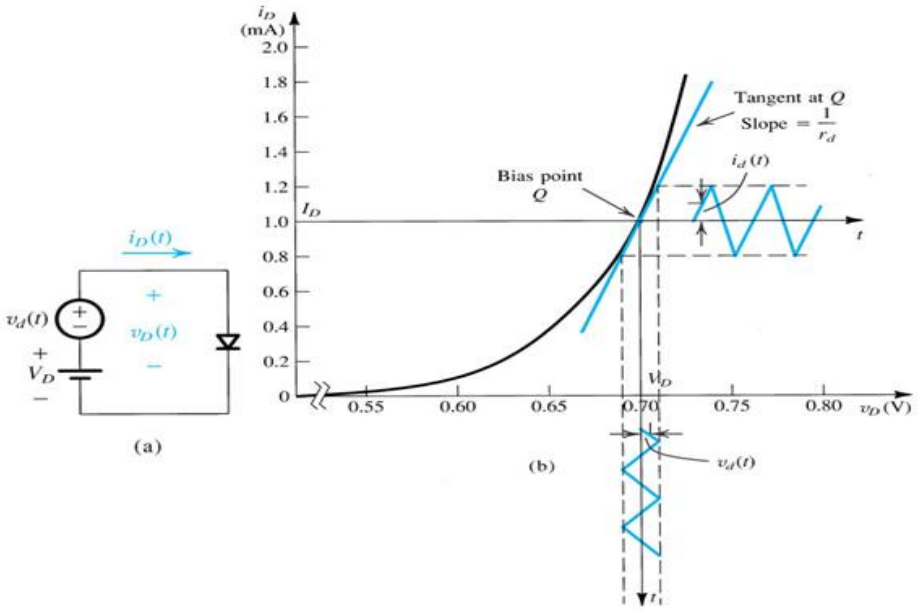


Fig. 2.7: Development of the diode small-signal model (for the diode with η=2)

- In the absence of the signal vd(t), the diode voltage and the corresponding dc current are given by

$$v_D = V_D \text{ and}$$

$$I_D = I_S\, e^{[V_D/\eta V_T]} \qquad \text{----------} \quad (2.1.4)$$

- When the signal $v_d(t)$ is applied, the total instantaneous diode voltage $v_D(t)$ and the

corresponding total instantaneous current are be given by

$$v_D(t) = V_D + v_d(t) \quad \text{---------- (2.1.5)}$$

$$i_D(t) = I_S\, e^{[v_D/\eta V_T]} \quad \text{---------- (2.1.6)}$$

- Substituting for v_D from equation (2.3.5) gives $i_D(t) = I_S\, e^{[(V_D + v_d)/\eta V_T]}$
  Which can be rewritten as $i_D(t) = I_S\, e^{[v_D/nV_T]}\ e^{[v_d/nV_T]} = I_D\, e^{[v_d/nV_T]}$ ----- (2.1.7)
- If the amplitude of the signal vd(t) is kept sufficiently small such that

  $[v_d / {}^{nV}{}_T] \ll 1$
- Then expansion of equation (2.1.7) in a series and truncate the series after the first two terms to obtain the approximate expression

$$i_D(t) \simeq I_D\left(1 + \frac{v_d}{nV_T}\right) \quad \text{---------- 2.1.8}$$

- This is the small-signal approximation. This approximation is valid for signal whose amplitudes are smaller than about 10 mV for the case n=2 and 5 mV for n=1.
- From equation (2.1.8) we have

$$i_D(t) \simeq I_D\left(1 + \frac{v_d}{nV_T}\right) \quad \text{----------2.1.9}$$

- Thus, superimposed on the dc current I_D, signal current component is directly proportional to the signal voltage v_d.

$$i_D = I_D + i_d \quad \text{---------- (2.1.10)}$$

where,

$$i_d = \frac{I_D}{nV_T} v_d$$

- The quantity relating the signal current i_d to the signal voltage v_d is called diode small-signal conductance (in mhos). The inverse of this parameter is the diode small-signal resistance or incremental resistance (r_d).

$$r_d = nV_T / I_D \quad \text{---------- (2.1.11)}$$

- The value of r_d is inversely proportional to the bias current I_D.
  From the Fig. 2.7 (b),

$$i_d = v_d / r_d \qquad r_d = 1 \Big/ \left[\frac{\partial i_D}{\partial v_D}\right]_{i_D = I_D}$$
$$r_d = nV_T / I_D \qquad \text{----------(2.1.12)}$$

- The small-signal model of diode forward characteristics and its equivalent circuit representation are shown in Fig. 2.8. After the dc analysis is performed, the small-signal equivalent circuit is obtained by eliminating all dc sources (i.e., short circuiting dc voltage sources and open-circuiting dc current sources) and replacing the diode by its small-signal resistance.

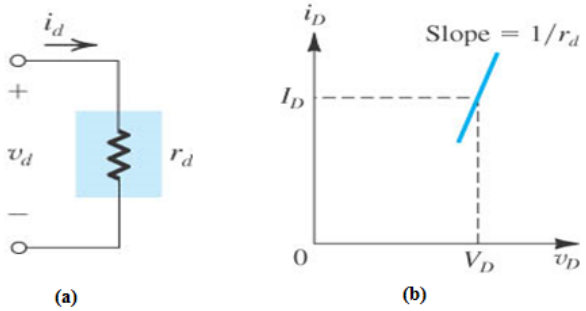


Fig. 2.8: The small-signal model of diode forward characteristics and its equivalent circuit representation.

ix) Use of diode forward drop in voltage regulation

- A voltage regulator is a circuit whose purpose is to provide a constant dc voltage between its output terminals.
- The output voltage is required to remain as constant as possible in spite of
  (a) changes in the load current drawn from the regulator output terminal and
  (b) changes in the dc power-supply voltage that feeds the regulator circuit.
- Since the forward voltage drop of the diode remains almost constant at approximately 0.7 V while the current through it varies by relatively large amounts, a forward-biased diode can make a simple voltage regulator.

2.2 Zener Diode

- Zener diode which are fairly popular for the voltage regulation. Voltage regulator is the circuits that provide constant d.c output voltages in the face of changes in their load current and in the system power voltage supplies.
- Zener diode sometimes referred as Breakdown diodes.

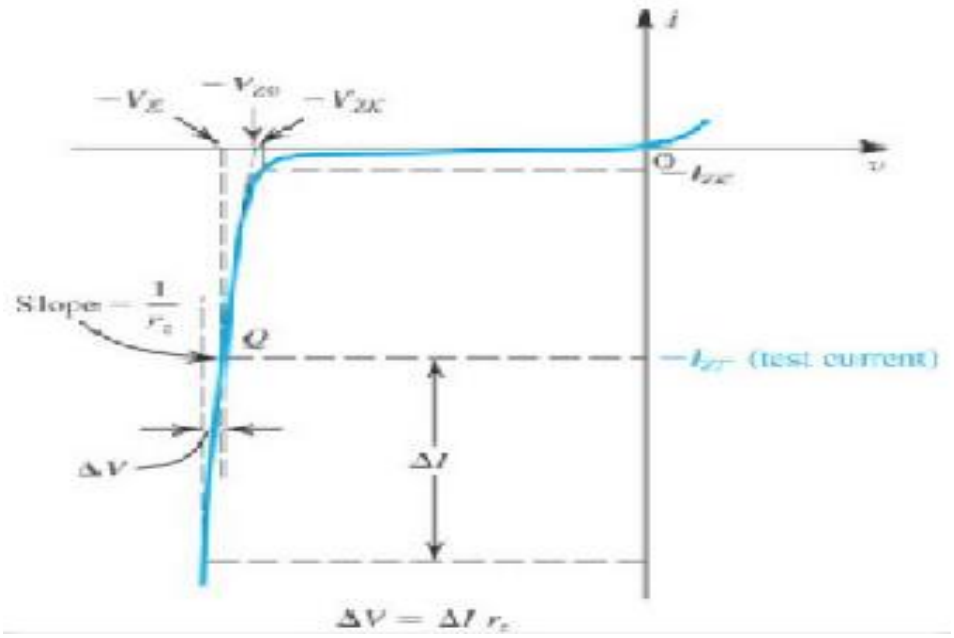


Fig. 2.9: The diode *i-v* characteristics in Breakdown region

Where, I_{zk} - Knee current and I_{zT} – Test current

V_z – Voltage across the zener diode

V_{zo} – the point at which the straight line of slope $1/r_z$ intersects the voltage axis

V_{zk} – Knee voltage

2.2.1 Specifying and modelling the Zener diode

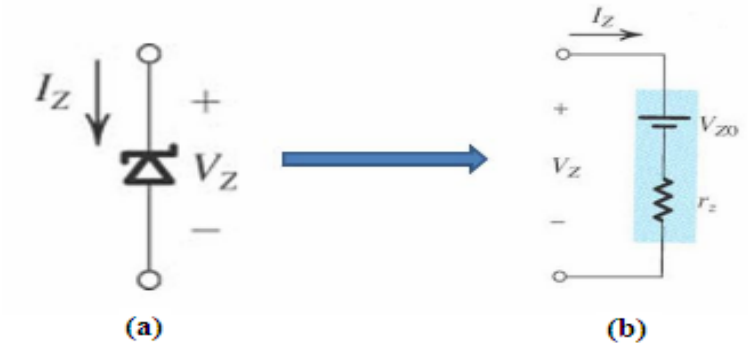


Fig. 2.10: a) Symbol of Zener diode; b) Models for the zener diode

$$V_Z = V_{Z0} + r_z I_Z$$

- $I_s = \frac{V_i - V_z}{R_s}; V_i >> V_z$
- $r_z = \Delta V_z / \Delta I_z$

2.2.2 Use of the Zener as a shunt voltage regulator

- A voltage regulator circuit using a zener diode is shown in Fig. 2.11. This circuit is called as a shunt regulator because the zener diode is connected in shunt to the load.
- Thw function of a regulator is to provide an output voltage V_0 that is as constant as possible in spite of the ripple in V_S and the variations in the load current $I_{L.}$
- Two parameters that can be used to measure regulation are line regulation and load regulation.
- Line regulation: It is defined as change in V_0 corresponding to a 1-V change in V_s

Line regulation = $\Delta V_0 / \Delta V_s$

- Load regulation: It is defined as change in V0 corresponding to a 1-mA change in I_L

Load regulation = $\Delta V_0 / \Delta I_L$

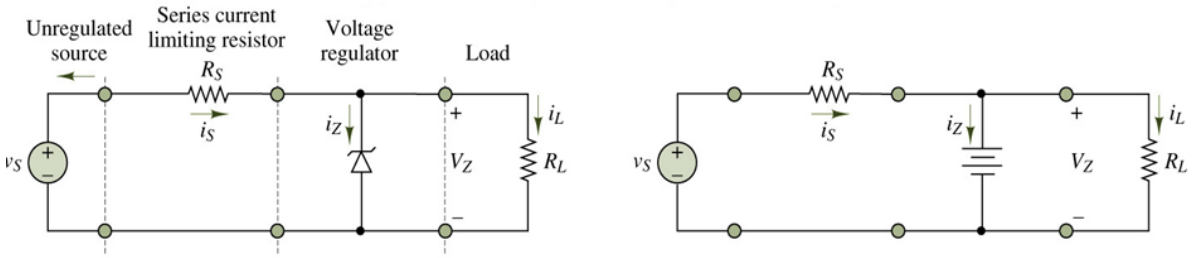


Fig. 2.11: a) Practical voltage regulator b) Simplified voltage regulator

2.2.3 Temperature effects

- The dependence of zener voltage V_Z on temperature is specified in terms of its temperature coefficient TC, or **temco** and is usually expressed in $mV/^0C$
- The value of TC depends on the zener voltage, and for a given diode the TC varies with the operating current.
- Zener diodes whose V_Z are lower than about 5V exhibit a negative TC and zener diode with higher voltages exhibits positive TC.

- The TC of a zener diode with a V_Z of about 5 V can be made zero by operating the diode at a specified current
- Another commonly used technique for obtaining a reference voltage with low temperature coefficient is to connect a zener diode with a positive TC of about 2 mV/^{0}C in series with a forward conducting diode
- Since the forward conducting diode has a voltage drop of 0.7 V and a TC of about -2 mV/^{0}C, the series combination will provide a voltage of (V_Z+0.7) with a TC of about 0.

2.3 SPICE models for p-n junction and Zener diodes

2.3.1 The diode model

- The more faithfully the model represents the various characteristics of the device, the more accurately the simulation results will describe the operation of an actual fabricated circuit.
- To see the effect of various imperfections in device operation on circuit performance, these imperfections must be included in the device model used by circuit simulator.
- The large-signal SPICE model for the diode is shown on above figure. The static behaviour is modeled by the exponential I-V relationship.

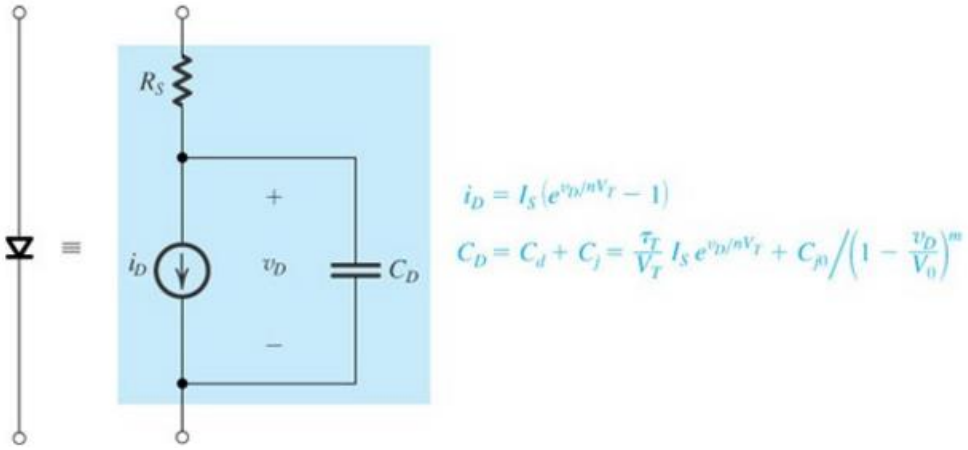


Fig. 2.12: SPICE model of a pn junction diode

- The dynamic behaviour is represented by the non- linear capacitance C_D, which is the sum of the diffusion C_d and the junction capacitance C_j. The series resistance Rs represents the total resistance of the p and n regions. The value of this resistance (R_s) is

practically zero. But it is typically a range of few ohms for small-signal diodes.

Table 2.1: Parameters of pn-junction diode

SPICE Parameter	Symbolic notation	Description	Units
IS	I_S	Saturation current	A
N	n	Emission coefficient	
RS	R_S	Ohmic resistance	Ω
VJ	V_0	Built-in potential	V
CJO	C_{j0}	Zero bias depletion (junction) capacitance	F
M	m	Grading coefficient	
TT	τ_T	Transit time	s
BV	V_{ZK}	Breakdown voltage	V
IBV	I_{ZK}	Reverse current at V_{ZK}	A

2.3.2 The Zener diode model

- The diode model shown in above figure does not adequately describe the operation of the diode in the breakdown region. Hence, it does not provide a satisfactory model for zener diode.
- However, the equivalent circuit model is shown below and it can be used to simulate a zener diode in SPICE.
- Here, diode D1 is an ideal diode which can be approximated in SPICE by using a very small value for n (say n=0.01). Diode D2 is a regular diode that models the forward bias region of the zener diode

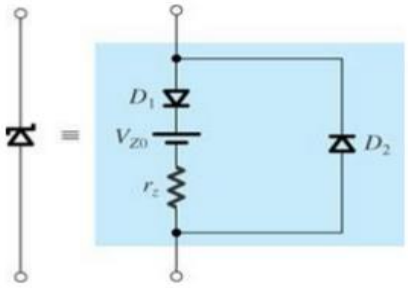


Fig. 2.13: SPICE diode model of zener diode

2.4 Applications of Diode

1. Diode logic gates

- Diodes together with resistors can be used to implement digital functions(logic functions).
- Consider a positive logic system in which voltage values close to 0 V corresponds to logic 0 (low level) and voltage values close to +5 V corresponds to logic 1 (high level).
- A three input OR gate and AND gate using diode logic is shown in fig. 2.14.

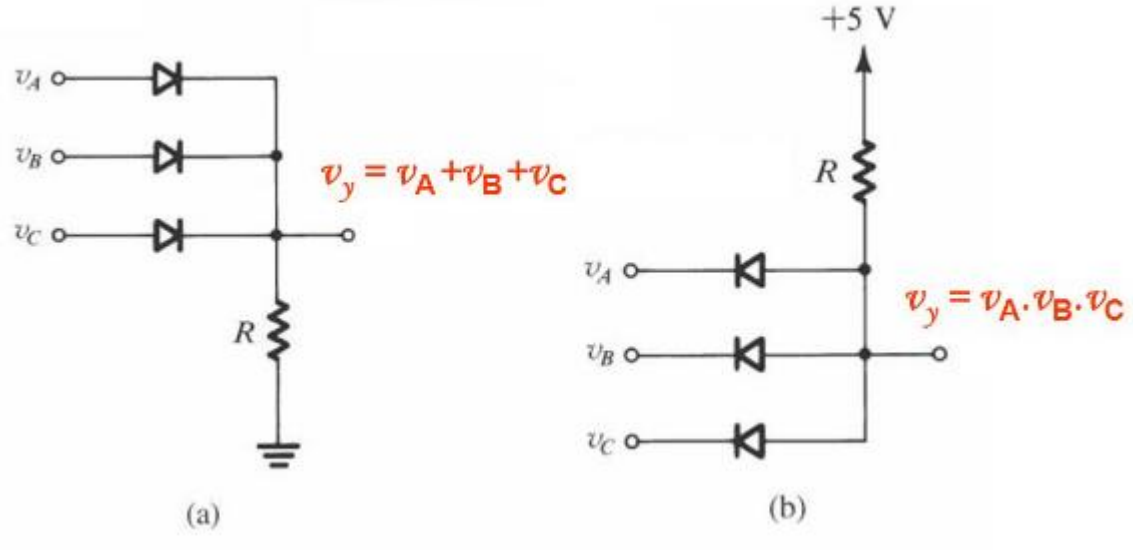


Fig. 2.14: Diode logic gates: (a) OR gate; (b) AND gate (in positive logic system)

- The circuit of **OR gate** has three inputs, v_A, v_B and v_C. The diodes connected to +5 V input will conduct thus clamping the output v_Y to a value equal to+5 V.
- This positive voltage at the output will keep the diodes cutoff (whose inputs are low). Thus the output will be high if one or more of the inputs are high. The circuit therefore implements the logic OR function, which in Boolean notation is expressed as, Y = A+B+C
- Similarly the same logic can be implemented **for AND gate**. In this circuit, if any input is held at a voltage equal to 0 V, corresponding diodes are shorted and the output clamps to 0 V.If all the inputs are held at logic high state, diodes will be cut-off and the output voltage is nearly equal to +5 V.
- The circuit therefore implements the logic AND function, which in Boolean notation is

expressed as, Y = A.B.C

2. Rectifier

- A fundamental application of the diode, one that makes use of its nonlinear *i-v* curve, is the rectifier circuit.

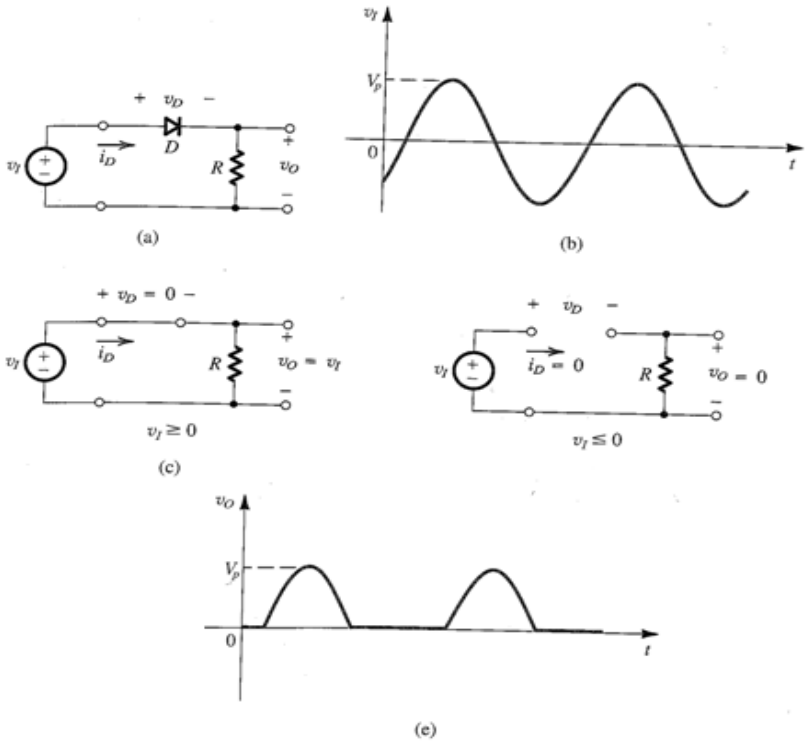


Fig. 2.15: (a) Rectifier circuit (b) Input waveform (c) Equivalent circuit when $v_i \geq 0$ (d) Equivalent circuit when $v_i \leq 0$ (d) Output waveform

- The circuit consists of the series connection of a diode D and a resistor R as shown in Fig. 2.15
- During the positive half-cycles of the input sinusoid, the positive V_i will cause current to flow through the diode in its forward direction. It follows that the diode voltage V_d will be very small (ideally zero). The output voltage V_0 will be equal to the input voltage V_i.
- During the negative half-cycles of V_i, the diode will not conduct and V_0 will be zero.
- While V_i alternates in polarity and has a zero average value but V_0 is unidirectional and has a finite average value or a dc component.

- Thus the circuit rectifies the signal and hence is called a Rectifier. Rectifier is used to generate dc from ac.

2.5 Rectifier circuits

- One of the applications of Diode is in the design of Rectifier circuit.
- A diode rectifier circuit is an essential building block of Power supplies required to power electronic equipment.

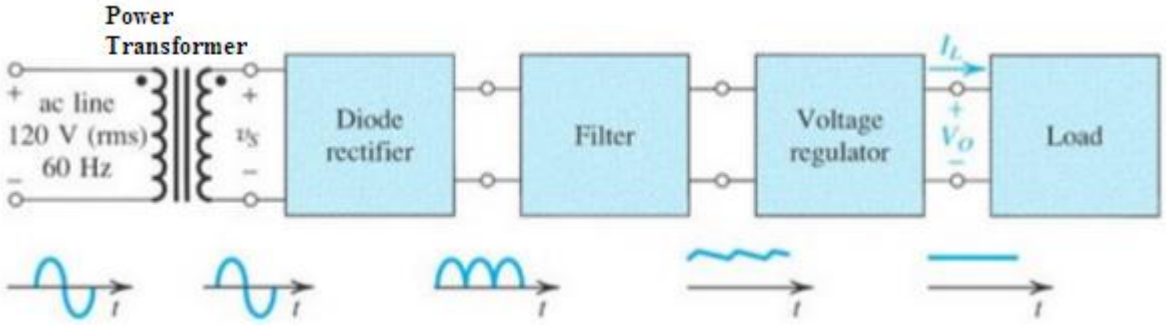


Fig. 2.16: Block diagram of a dc power supply

- To achieve its purpose a power supply must:
  - Step down transformer is used to step down the magnitude of the voltages Ac voltage
  - Convert AC to Pulsating DC (non-zero average or DC component) using rectifiers like Half-wave & Full-wave rectifiers.
  - Use the filters to reduce the Ripples in rectifier output (time dependent component)
  - Use Regulators to stabilize filter output voltage against the supply voltage and change in load variations.

2.5.1 Half wave Rectifier

- It is a simplest process used to convert ac to dc.
- A diode is used to clip the input signal excursions of one polarity to zero.
- In half-wave rectifier circuit mains voltage (220 to 240 V) is applied to the primary of a step-down transformer. The secondary of transformer steps down the 240 V r.m.s. to 12 V r.m.s.
- The Diode will be forward biased during each positive half-cycle of input hence current flows from cathode to anode of the diode. In forward bias diode behaves like a closed

switch.

- The circuit current flows in the opposite direction, when the voltage bias across the diode will be reversed, causing the diode to act like an open switch.
- The switching action of diode results in a pulsating output voltage which is developed across the load resistor R.

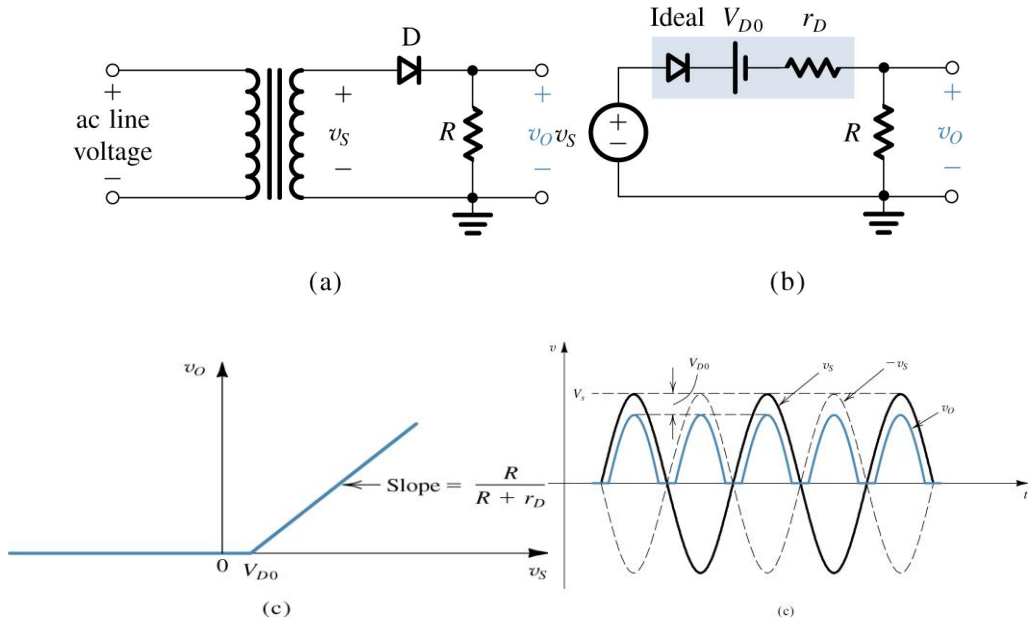


Fig. 2.17: a).Half wave rectifier; b) Equivalent circuit of half wave rectifier with diode replaced with battery and resistor model; c) Transfer characteristics of rectifier circuit; d) Input and output waveforms

- From the fig. 2.17(b) we can write

$$v_O = 0, \qquad v_S < V_{D0}$$

$$v_O = \frac{R}{R + r_D} v_S - V_{D0} \frac{R}{R + r_D}, \qquad v_S \geq V_{D0}$$

- Transfer characteristics represented equations is shown in fig
- In many applications $r_D << R$ .hence equation 2 simplified as

$$v_O \simeq v_S - V_{D0}$$

V_{Do} = 0.7V or 0.8V

- **Peak Inverse voltage (PIV):** The diode must be able to withstand without damage under applied reverse bias voltage. PIV is one of the important parameter of the rectifier circuit.

- When V_s is negative in figure(a) the diode will be cut-off and $V_o = 0$

2.5.2 Full wave Rectifier

- A Full Wave Rectifier is a circuit, which converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conducts during one half cycle while the other conducts during the other half cycle of the applied. ac voltage.
- Center tapped transformer is used to provide 2 equal input voltages.

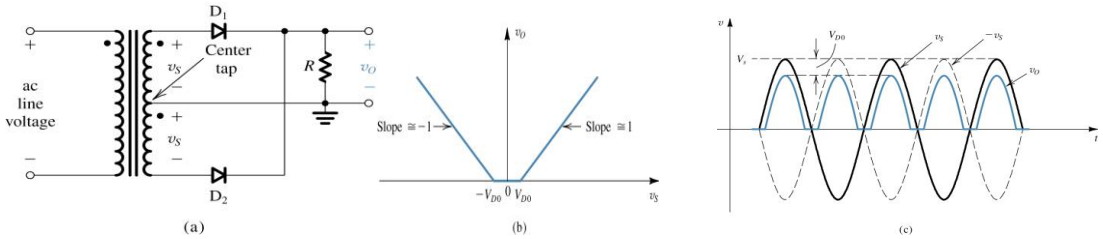


Fig. 2.18: a) Full wave rectifier; b) Transfer characteristics of rectifier circuit; c) Input and output waveforms

- To find the PIV of the diodes in the full-wave rectifier circuit, consider the situation during the positive half-cycles. Diode D_1 is conducting, and D_2 is cut-off. The voltage at the cathode of D_2 is v_0, and that at anode is $-vs$. Thus the reverse voltage across D_2 will be (V_0+V_s), which will reach its maximum when v_0 is at its peak value of $(V_S - V_D)$, and v_s is at its peak value of V_S; thus

$$\mathbf{PIV= 2V_S - V_D}$$

2.5.3 Bridge Rectifier

- Another type of circuit that produces the same output waveform as the full wave rectifier circuit is the **Full Wave Bridge Rectifier**.
- This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output.
- The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost.
- The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

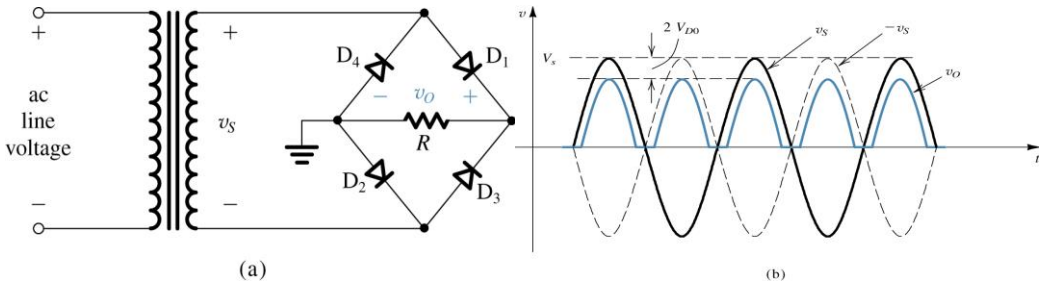


Fig. 2.19: a) Bridge Rectifier circuit diagram; b) Input, Output forms

- To determine the peak inverse voltage of each diode, consider circuit during the positive half cycle. Then the reverse voltage across the D_3 is from the fig. 2.19(a)

$$v_{D3}\ (\text{reverse}) = v_O + v_{D2}\ (\text{forward})$$

- The maximum value of V_{D3} occurs at the peak of V_o and is given by

$$\text{PIV} = V_s - 2V_D + V_D = V_s - V_D$$

- PIV of bridge rectifier is about half the value of center taped rectifier.

2.5.4 Comparison of Rectifiers

Table 2.2: Comparison of various rectifiers

Parameters	**HWR**	**FWR (CT)**	**FWR (BR)**
V_{DC}	V_m/π	$2V_m/\pi$	$2V_m/\pi$
V_{rms}	$V_m/2$	$V_m/\sqrt{2}$	$V_m/\sqrt{2}$
γ **Ripple factor**	1.21	0.482	0.482
η **Rectification efficiency**	40.6%	81%	81%

PIV **Peak Inverse Voltage**	V_m	$2V_m$	V_m

2.5.5 Full wave rectifier with capacitor filter (peak rectifier)

- The property of capacitor is that it allows ac component and blocks the dc component. The operation of capacitor filter is to short the ripple to ground but leave the dc to appear at the output when it is connected across a pulsating dc voltage.

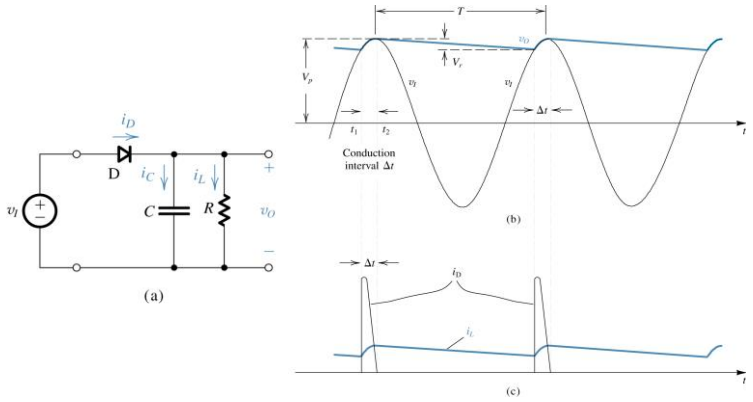


Fig. 2.20: a) Circuit diagram of full wave rectifier with capacitor filter; b) Voltage and current waveforms in waveforms in peak rectifier.

- To analyze the circuit in figure (a) take the assumption RC >> T and observe the steady state input and output waveforms in fig. 2.20(c)
- The waveform of the load current

$$i_L = v_O / R$$

- Diode current when conducting

$$i_D = i_C + i_L$$
$$= C\frac{dv_I}{dt} + i_L$$

- The diode conducts for a brief interval, Δt near the peak of the input sinusoid and supplies the capacitor with charge equal to that lost during the much longer discharge interval. The latter is approximately equal to the period *T*
- Assuming an ideal diode, the diode conduction begins at time t_1, at which the input v_1

equals the exponentially decaying output v_0. Conduction stops at t_2 shortly after the peak of v_i; the exact value of t_2 can be determined by setting $i_D = 0$.

- During the diode-off interval, the capacitor, C discharges through R, and thus v_0 decays exponentially with a time constant 'RC'. The discharge interval begins just past the peak of v_1. At the end of the discharge interval, which lasts for almost the entire period T, $v_0 = V_p - V_r$, where, V_r is the peak to peak ripple voltage. When RC >> T, the value of Vr is small.
- When V_r is small, v_0 is almost constant and equal to the peak value of v_1. Thus the dc output voltage is approximately equal to Vp. Similarly, the current i_L is almost constant, and its dc component I_L is given by

$$I_L = V_p / R$$

- If desire, a more accurate expression for the output dc voltage can be obtained by taking the average of the extreme values of *v0*,

$$V_0 = V_p - (1/2).\ V_r$$

- With these observations, Vr will be derived and the average and peak values of the diode current. During the diode off interval, V0 can be expressed as

$$\boldsymbol{V_0 = V_p.e^{-t/RC}}$$

- At the end of the discharge interval,

$$V_p - V_r = V_p.\ e^{-T/RC}$$

Now, since RC >> T , we can use the approximation $e^{-T/RC} = 1-T/RC$ to obtain

$$V_r \simeq V_p \frac{T}{CR}$$

- The ripple voltage in terms of frequency

$$V_r = \frac{V_p}{fCR} \quad , \qquad V_r = \frac{I_L}{fC}$$

- We can determine the conduction interval, Δt from

$$V_p \cos(\omega \Delta t) = V_p - V_r$$

Where, $\omega = 2\pi f = 2\pi/T$ is the angular frequency of v_1. Since (ω Δt) is a small angle, we can employ the expression $\cos(\omega \Delta t) \approx 1-1/2\ (\omega \Delta t)^2$ to obtain

$$\boldsymbol{\omega \Delta t \approx (2\ Vr/\ Vp)^{1/2}}$$

Note that Vr<< Vp, the conduction angle ω Δt will be small as assumed

To determine the average diode current during conduction, i_{Dav} , we relate the charge that

the diode supplies to the capacitor

$$Q_{\text{supplied}} = i_{C\text{av}}\,\Delta t$$

$$i_{C\text{av}} = i_{D\text{av}} - I_L$$

- To discharge the capacitor loses during the discharge interval

$$Q_{\text{lost}} = CV_r$$

$$i_{D\text{av}} = I_L(1 + \pi\sqrt{2V_p/V_r})$$

- Observe that Vr << Vp the average diode current during conduction is much greater than the dc load current.
- Assuming that I_L almost constant, we obtain

$$i_{D\text{max}} = I_L(1 + 2\pi\sqrt{2V_p/V_r})$$

Waveform of i_D is almost right angle triangle.

- The accuracy of the results can be improved by taking the diode drop into consideration. This can be easily done by replacing the peak voltage V_p to which the capacitor charges with (V_p-V_D) for half-wave circuit and full-wave circuit using a center-tapped transformer and with (V_p-2V_D) for the bridge rectifier.
- The peak rectifier circuits find application in signal processing systems where it is required to detect the peak of an input signal. In such a case the circuit is referred to as a **peak detector.**
- A particularly popular application of the peak detector is in the design of a demodulator for amplitude-modulated signals.

2.5.6 The precision half-wave rectifier – the super diode

- The **precision rectifier**, also known as a **super diode**, is a configuration obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. It is useful for high-precision signal processing.
- The rectifier circuits suffer from one or two diode drops in the signal paths. Thus these circuits work well only when the signal to be rectified is much larger than the voltage drop of conducting diode (0.7 V or so).
- Where the signal to be rectified is small (e.g., on order of 100 mv or so) and thus clearly insufficient to turn on a diode. Also, in instrumentation applications, the need arises for rectifier circuits with very precise and predictable transfer characteristics. The basic

circuit implementing such a feature is shown in below figure. Where, R_L can be any load..

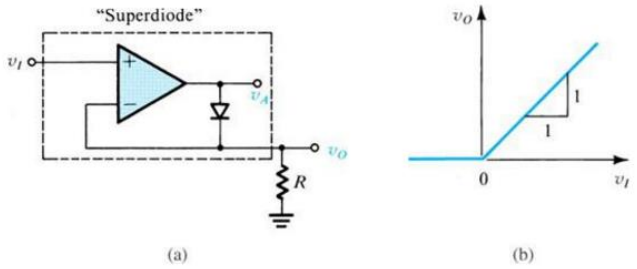


Fig. 2.21: a) Precision half wave rectifier circuit; b) Transfer characteristics of zener diode

- When the input voltage is negative, there is a negative voltage on the diode, so it works like an open circuit, no current flows through the load, and the output voltage is zero
- When the input is positive, it is amplified by the operational amplifier which switches the diode on. Current flows through the load and, because of the feedback, the output voltage is equal to the input voltage.
- The actual threshold of the super diode is very close to zero, but is not zero. It equals the actual threshold of the diode, divided by the gain of the operational amplifier.
- The transfer characteristics of this circuit are almost identical to the ideal characteristics of a half wave rectifier.

2.6 Limiting (or) Clippers And Clamping Circuits

- Use of diodes along with resistor and capacitors to shape wave forms
- If we want to clip portion of the waveform we use clippers for this purpose and if we want to shift or clamp the dc voltage level we use clampers.

Clippers (Limiting) : clippers are networks that use diodes to clip a portion of input signal without distorting the remaining part of the wave form.

Clampers : A clamper is a network constructed of diodes, a resistor and capacitor that shift the waveform to a different dc level without changing the appearance of the applied signal.

2.6.1 Limiting Circuits (or) Clipper circuit

- Clippers are further divided into series and parallel clippers.
- Within series and parallel there is biased and un biased clippers.

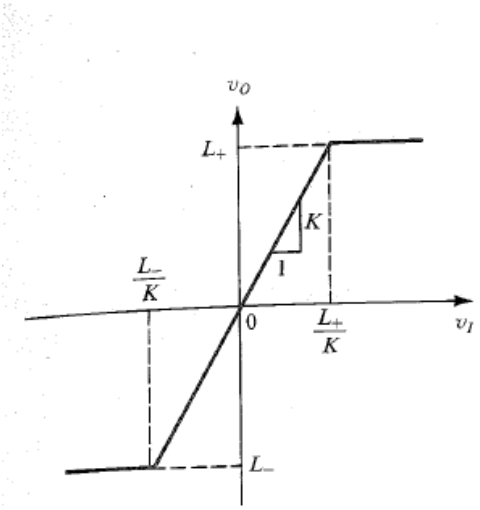


Fig. 2.22 General transfer characteristic for a limiter circuit

- Fig 2.22 shows the general transfer characteristics of a limiter circuit.
- As indicated for inputs in a certain range $L_- / K \leq V_I \leq L_+ / K$,
- The limiter act as a linear circuit providing an output proportional to the input, Vo =K V_I. In general K >1.
- If K≤1 and are known as passive limiters
- If V_I exceeds the upper threshold (L_+ / K), the output voltage is limited or clamped to the upper limiting level L_+
- on the other hand , If V_I reduced below the lower limiting threshold (L_- / K), the output voltage is limited or clamped to the upper limiting level L_-
- The above fig describes a double limiter i.e. a limiter that works on both the positive and negative peaks of an input wave form as shown in below fig 2.23

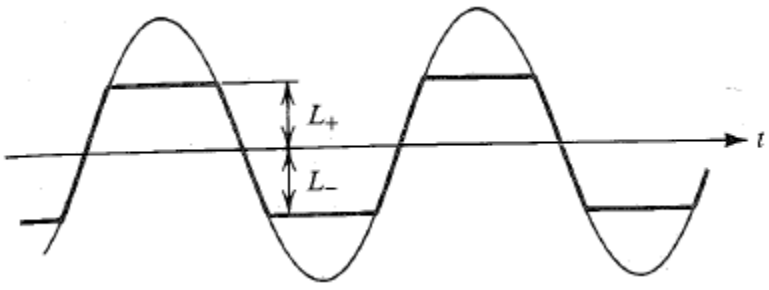


Fig. 2.23 Applying a sine wave to a limiter cn result in clipping off its two peaks

- Limiters find applications in a variety of signal processing systems, and op-amps.

2.6.2 The Clamped Capacitor or DC Restorer

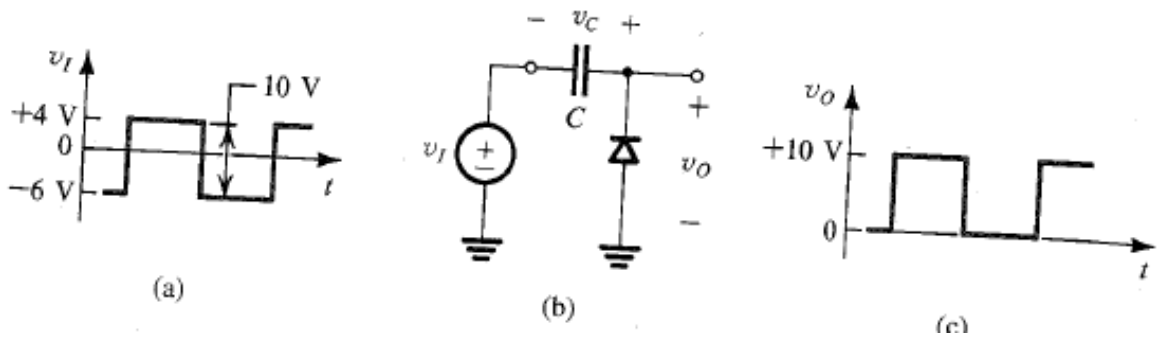


Fig. 2.24 The clamped capacitor or dc restore with a square-wave input and no load

- If in the basic rectifier circuit the output is taken across the diode rather than across the capacitor , an interesting circuit with important application results.
- The circuit called a dc restorer as shown in fig. 2.24 fed with a square wave.
- The polarity in which the diode is connected , the capacitor will charge to a voltage Vc with the polarities indicated in fig. and equal to magnitude of the most negative peak of the input voltage.
- subsequently the diode turns off and the capacitor retains its voltage indefinitely.
- if, for instance the inpur square wave has the arbitrary level -6 V, then Vc will equal to 6 V. The output voltage Vo is given by Vo= Vf+ Vc
- In above example the output will be a square wave with levels of 0 V and +10 V.

2.6.3 The Voltage Doubler

- Below fig.2.25 shows a circuit composed of two section in cascade.
- a clamp formed by C_1 and D_1 and a peak rectifier formed by D_2 and C_2
- When excited by a sinusoid of amplitude V_p the clamping section provide the voltage waveform shown in below fig. Assuming ideal diodes.
- The positive peaks are clamped to 0 V , the negative peak reaches to $-2V_p$.
- In response to this waveform the peak detector section provides across capacitor

C_2 a negative dc voltage magnitude $2V_p$.

- The output voltage is double the input peak, the circuit is known as voltage doubler.

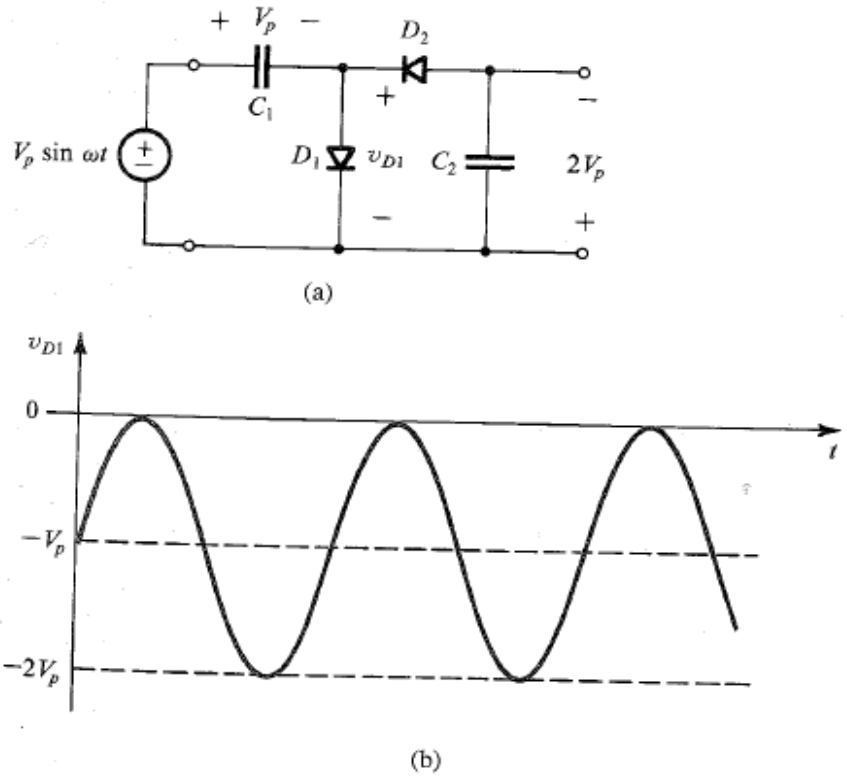


Fig2.25 : Voltage doubler (a) Circuit (b) Waveform of the voltage across D1

Assignment-Cum-Tutorial Questions

A. Questions testing the remembering / understanding level of students

I) Objective Questions

1. Sketch the I-V characteristics of an ideal diode.
2. Draw the three-input AND gate using diodes.
3. Write the applications of the diode.
4. Give the diode forward I-V relation.
5. For a decade change in current, the diode voltage changes by…….(from diode I-V equation)
6. Explain how zener diode acts as voltage regulator.
7. What is the PIV of diode in full-wave rectifier?
8. What is the PIV of diode in half-wave rectifier?
9. What is the PIV of diode in bridge rectifier?
10. What is the use of voltage regulators in Power supplies?
11. What is the suitable situation to use the small signal model ?
12. A diode for which you can change the reverse bias, and thus vary the capacitance is called as..... [ ]

    a) Tunnel diode b) Varactor diode c) Zener diode d) Switching diode

13. Which type of transformer is required to create a 180 degree input to a rectifier?
14. What is the basic principle behind the LED?
15. What is the difference between LED and photo diode?
16. The Schottky diode is used…… [ ]

    a) in high power circuits b) in circuit requiring negative resistance

    c) in very fast switching circuits d) in power supply rectifiers

17. What is the effect of temperature on Zener breakdown voltage
18. Precision rectifier is also called as .....
19. Draw the SPICE diode model.
20. Define clippers
21. define clampers

***II) Descriptive* Questions**

1. Sketch and explain the terminal characteristics of a diode.
2. Explain the operation of diode in forward and reverse bias region
3. Draw and explain various diode models in forward bias.
4. With the help of circuit diagram and waveforms, explain the operation of a diode half wave peak rectifier.
5. With the help of circuit diagram and waveforms, explain the operation of a center-tapped full-wave rectifier with shunt capacitive filter.
6. With the help of circuit diagram and waveforms, explain the operation of a Bridge rectifier.
7. Explain the operation of Zener diode and it's application.
8. Briefly discuss about varactor diode.
9. Explain the principle of operation of Schottky barrier diode
10. Explain the principle of operation of photo diode
11. Explain the principle of operation of Light Emitting Diode (LED)
12. Sketch & explain the SPICE diode & zener diode models.
13. Explain the voltage doubler

B. Question testing the ability of students in applying the concepts.

I) Objective Questions

1. Compute the values of I and V in the figure 2.1 (Diodes used are ideal).

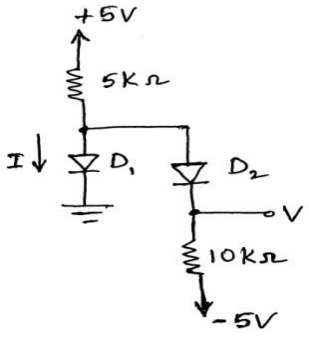


Fig. 2.1

2. A silicon diode said to be a 1rnA device displays a forward voltage of 0.7 V at a current of 1 mA. Evaluate the junction scaling constant I_s in the event that n is either 1 or 2. What

scaling constants would apply for 1 A diode of the same manufacture that conducts 1 A at 0.7 V?

3. A junction diode is operated in a circuit in which it is supplied with a constant current I. What is the effect on the forward voltage of the diode if an identical diode is connected in parallel? Assume $\eta = 1$.
4. Assuming the diodes to be ideal, find the values of I and V in the circuits shown in fig.2.2

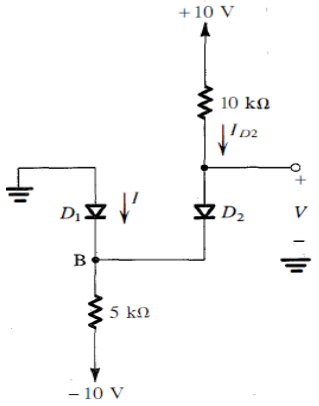


Fig. 2.2

5. The circuit shown in fig.2.3 can be used in a signaling system using one wire plus a common ground return. At any moment, the input has one of three values: +3 V, 0 V, -3 V. What is the status of the lamps for each input value?

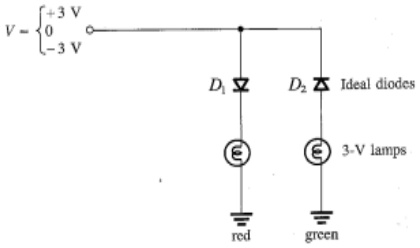


Fig. 2.3

6. If the output voltage of a bridge rectifier is 100 V. What will be the PIV of the diode?
7. A shunt regulator utilizing a zener diode with an incremental resistance of 5 Ω is fed through an 82 Ω resistor. If the raw supply changes by 1.3 V, what is the corresponding change in the regulated output voltage?
8. Assuming the diodes to be ideal, find the values of I and V in the circuits shown in fig 2.4

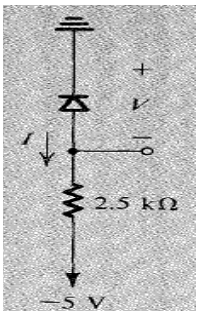


Fig. 2.4

9. Find the correct match between Group 1 and Group 2 :

Group 1	Group 2
(E) Varactor diode	(1) Voltage reference
(F) PIN diode	(2) High frequency switch
(G) Zener diode	(3) Tuned circuits
(H) Schottky diode	(4) Current controlled attenuator

10. Match items in Group 1 with items in Group 2, most suitably.

Group 1		Group 2	
P	LED	1	Heavy doping
Q	Avalanche photodiode	2	Coherent radiation
R	Tunnel diode	3	Spontaneous emission
S	LASER	4	Current gain

II) Descriptive Questions

1. A single-phase full-wave rectifier use semiconductor diodes. The transformer voltage is 6Vrms to center tap. The load consists of a 40 μF capacitor in parallel with a 250Ω resistor. The diode and the transformer resistances and leakage reactance may be neglected. Assume that the power-line frequency is 50 Hz. Calculate
   i) The dc current I_{dc} in the circuit.
   ii) Peak-to-peak amplitude of the ripple voltage, Vr
   iii) Ripple factor of a rectifier-filter output, r.
   iv) Percentage regulation
2. Use the iterative-analysis procedure to determine the diode current and voltage in the circuit shown below fig 2.5 for V_{DD} =1 V, R = 1 kΩ, and a diode having I_S= 10^{-15}A and η = 1

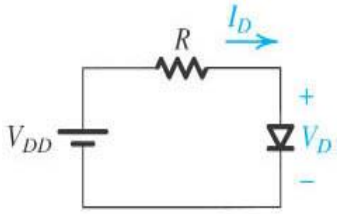


Fig. 2.5

3. For the logic gate shown in fig.2.6, assume ideal diodes and input voltage levels of 0 V and +5 V. Find a suitable value for R so that the current required from each of the input signal sources does not exceed 0.1mA.

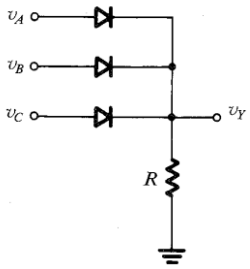


Fig. 2.6

4. For the rectifier circuit shown in fig 2.7, let the input sine wave have 120V rms value and assume the diode to be ideal. Select a suitable value for R so that the peak diode current does not exceed 50mA. What is the greatest reverse voltage that will appear across the diode?

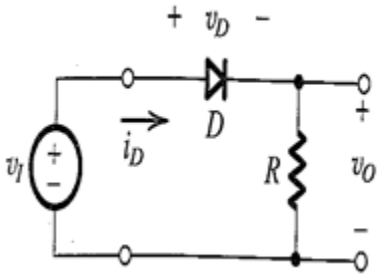


Fig. 2.7

5. (a) Solve the problems in Fig.2.8 using the constant voltage-drop (V_D= 0.7 V) diode model.

   (b) For the circuits shown in Fig. 2.8, using the constant voltage-drop (V_D= 0.7 V) diode, find the voltages and currents indicated.

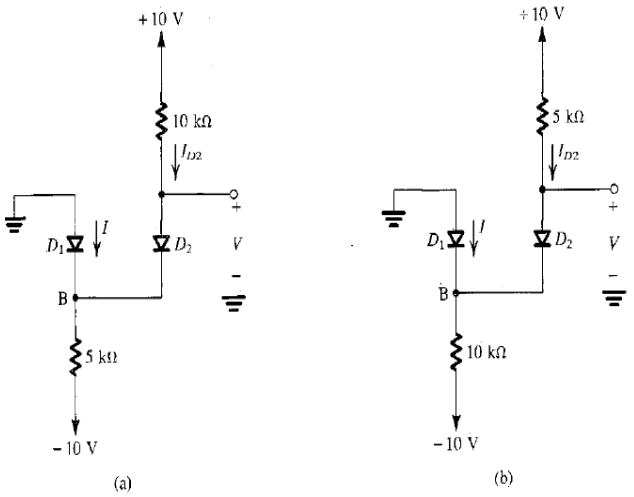


Fig. 2.8

6. Listed below are the results of measurements taken on several different junction diodes. For eaqch diode, the data provided are the diode current I, the corresponding diode voltage V, and the diode voltage at a current I/10. In each case, estimate I_s, n, and the diode voltage at 10 I.

   (a) 10 mA, 700 mV, 600 mV (b) 1 mA, 700 mV, 600 mV

7. Consider a peak rectifier fed by a 50 Hz sinusoid having a peak value V_p= 100 V. Let the load resistance R = 10 KΩ. Find the value of the capacitance C that will result in a peak-to-peak ripple of 2 V. Also, calculate the fraction of the cycle during which the diode is conducting and the average and peak values of the diode current.
8. For the half-wave rectifier circuit, let the input sine wave have 220 V rms value and assume the diode to be ideal. Select a suitable value for R so that the peak diode current does not exceed 50 mA. What is the greatest reverse voltage that will appear across the diode?
9. For the circuit shown in fig.2.9, both diodes are identical, conducting 10 mA at 0.7 V and 100 mA at 0.8 V. Find the value of R for which V = 80 mV.

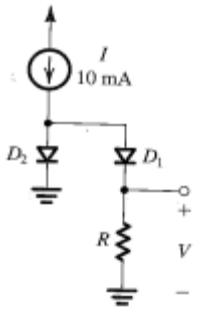


Fig. 2.9

10. A designer requires a shunt regulator of approximately 20 V. Two kinds of zener diodes are available: 6.8 V devices with r_z of 10 Ω and 5.1 V devices with r_z of 30 Ω. For the two major choices possible, find the load regulation. In this calculation neglect the effect of the regulator resistance R.

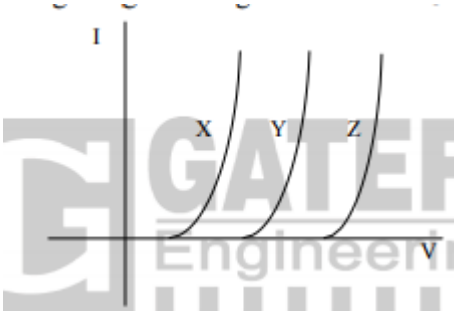
III) Creative Questions

1. Assuming the availability of diodes for which v_D = 0.7 V at i_D = 1 rnA and n = 1, design a circuit that utilizes four diodes connected in series, in series with a resistor R connected to a 10 V power supply. The voltage across the string of diodes is to be 3.0 V.
2. Design a diode voltage regulator to supply 1.5 V to a 150 Ω load. Use two diodes specified to have a 0.7 V drop at a current of 10 rnA and n = 1. The diodes are to be connected to a +5 V supply through a resistor R. Specify the value for R.
   a. What is the diode current with the load connected?
   b. What is the increase resulting in the output voltage when the load is disconnected?
   c. What change results if the load resistance is reduced to 100 Ω, 75 Ω and 50 Ω?
3. A designer requires a shunt regulator of approximately 20 V. Two kinds of zener diodes are available: 6.8 V devices with r_z of 10 Ω and 5.1V devices with r_z of 30 Ω. For the two major choices possible, find the load regulation. In this calculation neglect the effect of the regulator resistance R.

4. Design a diode voltage regulator to supply 1.5 V to a 150 Ω load. Use two diodes specified to have a 0.7 V drop at a current of 10 mA and n=1. The diodes are to be connected to a +5 V supply through a resistor R. Specify the value for R. What is the diode current with the load connected? What is the increase resulting in the output voltage when the load is disconnected?

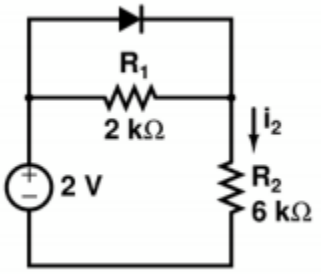
GATE previous questions

1. The I-V characteristics of three types of diodes at the room temperature, made of semiconductors X, Y and Z, are shown in the figure. Assume that the diodes are uniformly doped and identical in all respects except their materials. If EgX, EgY and EgZ are the band gaps of X, Y and Z, respectively, then [ ] (GATE 2015)



(A) EgX > EgY > EgZ (B) EgX = EgY = EgZ
(C) EgX < EgY < EgZ (D) no relationship among these band gaps exists

2. Assume that the diode in the figure has V_{on}= 0.7 V, on but is otherwise ideal. The magnitude of the current i_2 (in mA) is equal to _____. (GATE 2016)

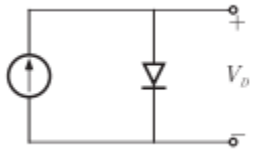


3. In a forward biased p-n junction diode, the sequence of events that best describes the mechanism of current flow is [ ] (GATE 2013)
(A) injection, and subsequent diffusion and recombination of minority carriers
(B) injection, and subsequent drift and generation of minority carriers
(C) extraction, and subsequent diffusion and generation of minority carriers
(D) extraction, and subsequent drift and recombination of minority carriers

4. A silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10ºC, the forward bias voltage across the PN junction [ ] (GATE 2011)
(A) increases by 60 mV (B) decreases by 60 mV

(C) increases by 25 mV (D) decreases by 25 mV

5. In the figure, silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20^0C V, D is found to be 700 mV. If the temperature rises to 40^0C V, D becomes approximately equal to…… [ ] (GATE 2008)



(A) 740 mV (B) 660 mV (C) 680 mV (D) 700 mV

3.MOS FIELD-EFFECT TRANSISTORS (MOSFETs)

Objective:

To analyze with the operation and characteristics of MOSFET

Syllabus:

MOSFETs: Device structure and physical operation - Operation with no gate voltage, Creating a channel for current flow, Applying a small v_{ds}, Operation as $v_{ds}$is increased, Derivation of the i_d-v_{ds} relationship, The p-channel MOSFET, Current-voltage characteristics - Circuit symbol, I_d-v_{ds} characteristics, Finite output resistance in saturation, Characteristics of the p-Channel MOSFET, The role of the substrate-the body effect, MOSFET operation as a switch, MOSFET operation as a linear amplifier, The depletion type MOSFET.

Outcomes:

At the end of the unit, student will be able to

- characterize the current flow in MOSFETs
- illustrate the effect of channel length modulation
- analyze the effect of substrate on device performance

Introduction

Compared to BJTs,

- MOSFETs can be made quite small (i.e., requiring a small area on the silicon IC chip)
- Their manufacturing process is relatively simple.
- Their operation requires comparatively little power.
- It is possible to pack large numbers of MOSFETs (>200 million) on a single IC chip, very-large-scale-integrated (VLSI) circuits such as those for memory and microprocessors.
- Analog circuits such as amplifiers and filters are also implemented in MOS technology, in smaller less-dense chips.
- Both analog and digital functions are increasingly being implemented on the same IC chip, in what is known as mixed-signal design.

3.1 Device structure and physical operation

3.1.1 Device Structure

- The transistor is fabricated on a *p-type* substrate, which is a single-crystal silicon wafer that provides physical support for the device.
- Two heavily doped n-type regions, indicated in the figure 3.1 as the n^+**source**and the n^+**drain**regions, are created in the substrate.
- A thin layer of silicon dioxide (Sio_2) of thickness t_{ox}(typically 2 - 50 nm), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions.
- Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the**body.**
- Thus four terminals are brought out: the gate terminal (G), the source terminal (S),the drain terminal (D), and the substrate or body terminal (B).Figure 3.1, shows the physical structure of the n-channel enhancement-type MOSFET.
- The name Metal Oxide Semiconductor FET is so because metal is not used for gate electrode. Most of modern MOSFETs are fabricated using silicon-gate technology, in

which a certain type of silicon, called poly-silicon, is used to form the gate electrode of MOSFET operation and characteristics applies irrespective of the type of gate electrode.

- Another name for the MOSFET is the insulated-gate FET or IGFET. This name also arises from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation thatcauses the current in the gate terminal to be extremely small (of the order of (of the order of 10^{-15} A).

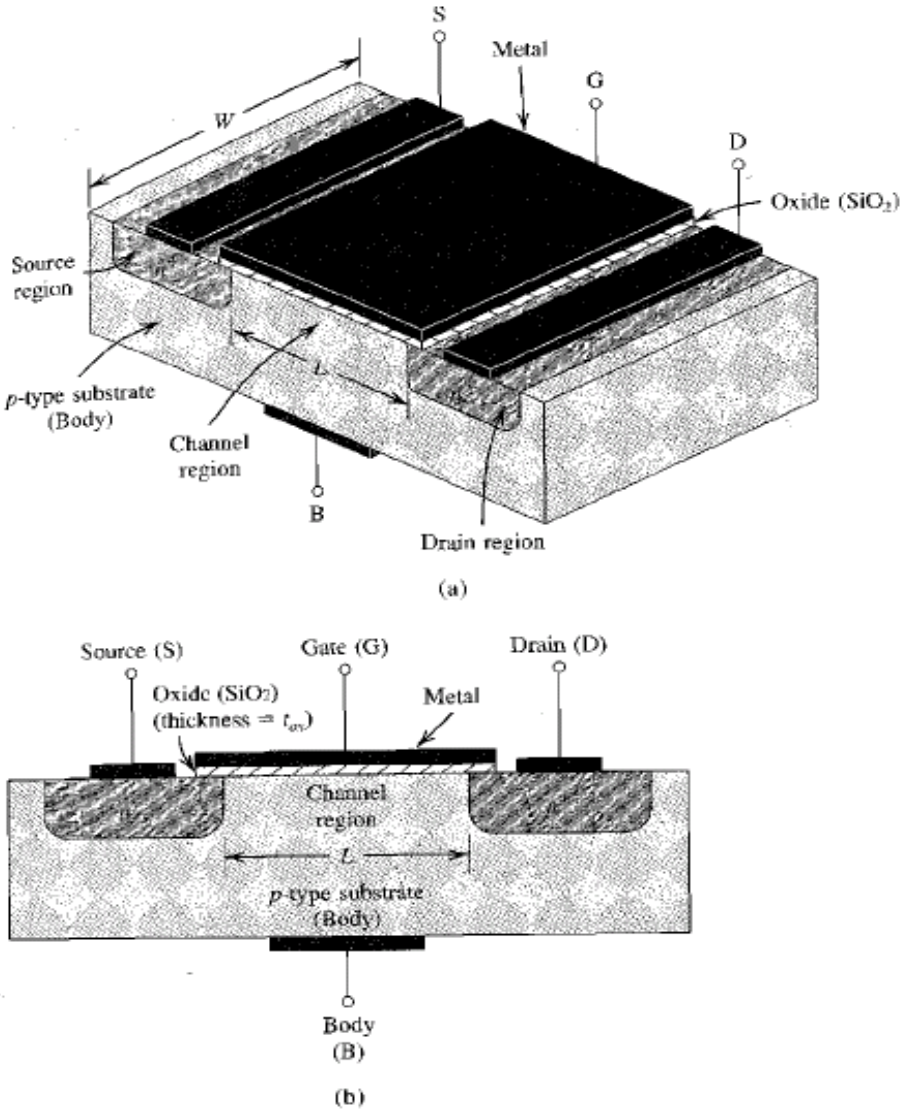


Fig. 3.1: Physical structure of the enhancement-type NMOS transistor: (a) perspective view (b) cross-section. Typically *L* = 0.1 to 3 μ*m*, *W*= 0.2 to 100 μ*m*, and the thickness of the oxide layer ($t_{ox}$is in the range of 2 nm to 50 nm).

- Observe that the substrate forms p-n junctions with the source and drain regions. In normal operation these p-n junctions are kept reverse-biased at all times.
- Since the drain will beat a positive voltage relative to the source, the two p-n junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal.
- Thus, here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a three-terminal device, with the terminals being the gate (G), the source (S), and the drain (D).
- It will be shown that a voltage applied to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labeled "channel region."
- This channel region has a length L and a width W, two important parameters of the MOSFET. Typically, L is in the range of 0.1 μm to 3 μm, and W is in the range of 0.2 μm to 100 μm.
- Finally, the MOSFET is a symmetrical device so that its source and drain can be interchanged with no change in device characteristics.

3.1.2 Operation with No Gate Voltage

- With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source.
- One diode is formed by the *p-n* junction between the n^+ drain region and the p-type substrate, and the other diode is formed by the *p-n* junction between the p-type substrate and the n^+source region.
- These back-to-back diodes prevent current conduction from drain to source when a voltage $v_{DS}$is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12}\,\Omega$).

3.1.3 Creating a Channel for Current Flow

- Assume when the source is grounded and thedrain and applied a positive voltage to the gate.
- Since the source is grounded, the gate voltageappears in effect between gate and source and thus is denoted v_{GS}. The positive voltage on the gate causes, the free holes (which are

positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region.

- The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate.
- As well, the positive gate voltage attracts electrons from the n + source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in effect created, connecting the source and drain regions, as indicated in Fig. 3.2.
- Now if a voltage isapplied between drain and source, current flows through this induced *n* region, carried bythe mobile electrons. The *induced n* region thus forms a channel for current flow from drainto source and *is aptly called so.* Correspondingly, the MOSFET of Fig. 3.2 is called an n-channel MOSFET or, alternatively, an NMOS transistor.
- An n-channelMOSFET is formed in a p-type substrate: The channel is created by *inverting* the substratesurface from *p* type to *n* type. Hence the induced channel is also called an inversion layer.

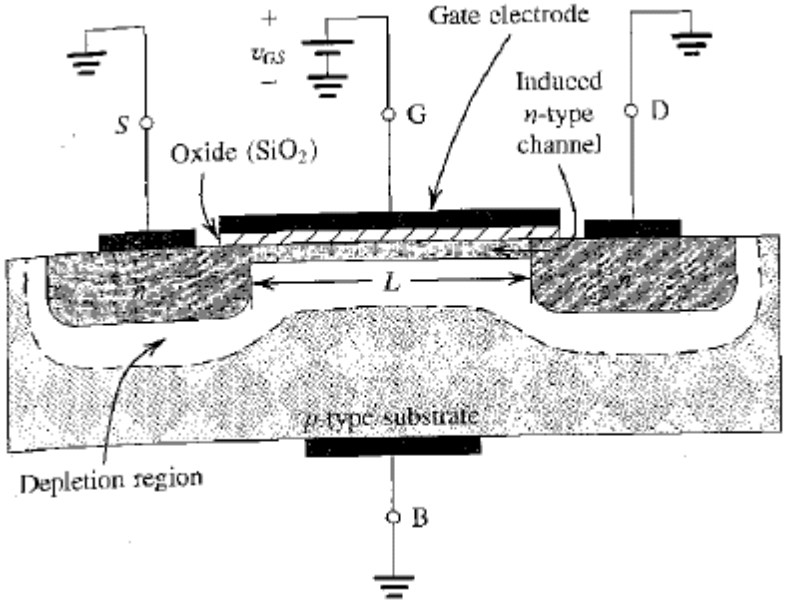


Fig.3.2:The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

- The value of v_{GS}at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t. $V_t$for an n-channel FET is positive. The value of $V_t$is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0 V.
- The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric.
- The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode).
- The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction.
- It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage $v_{DS}$is applied.

3.1.4 Applying a Small V_{DS}

- Having induced a channel, if we apply a positive voltage V_{DS} between drain and source, as shown in Fig.3.3. Consider the case where $v_{DS}$is small (i.e., 50 mV or so).
- The voltage v_{DS}causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain (hence the names source and drain). By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D, will be from drain to source, as indicated in Fig. 3.3.
- The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of V_{GS}. Specifically, for $V_{GS} = V_t$, the channel is just induced and the current conducted is still negligibly small.

- As v_{GS} exceeds V_t more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or, equivalently, reduced resistance.
- In fact, the conductance of the channel is proportional to the excess gate voltage (v_{GS} - V_t), also known as the **effective voltage** or the **overdrive voltage.** It follows that the current $i_D$will be proportional to (v_{GS} - V_t)and, to the voltage v_{DS}that causes $i_D$to flow.

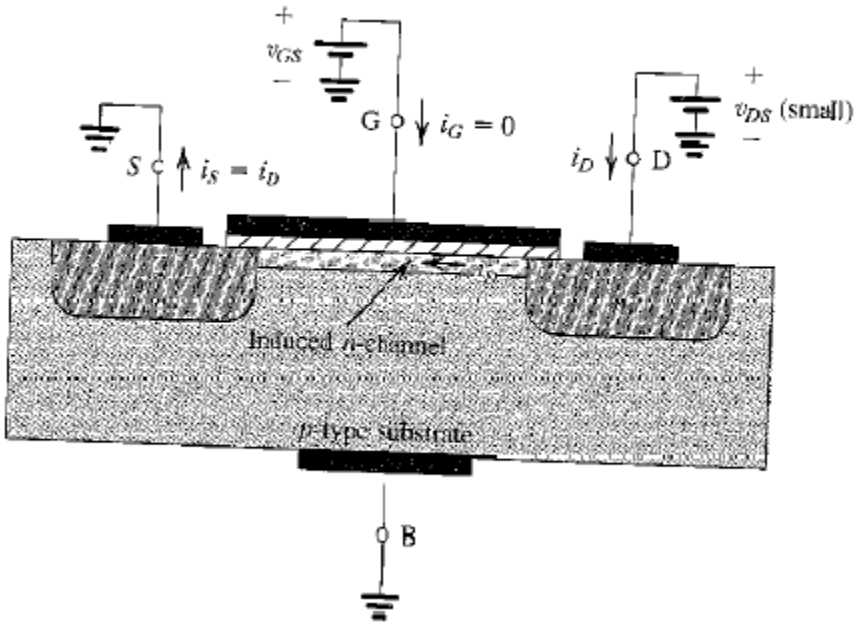


Fig.3.3: An NMOS transistor with $v_{GS}>V_t$, and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to (v_{GS}- V_t)and thus $i_D$is proportional to (v_{GS} - V_t)v_{DS}.

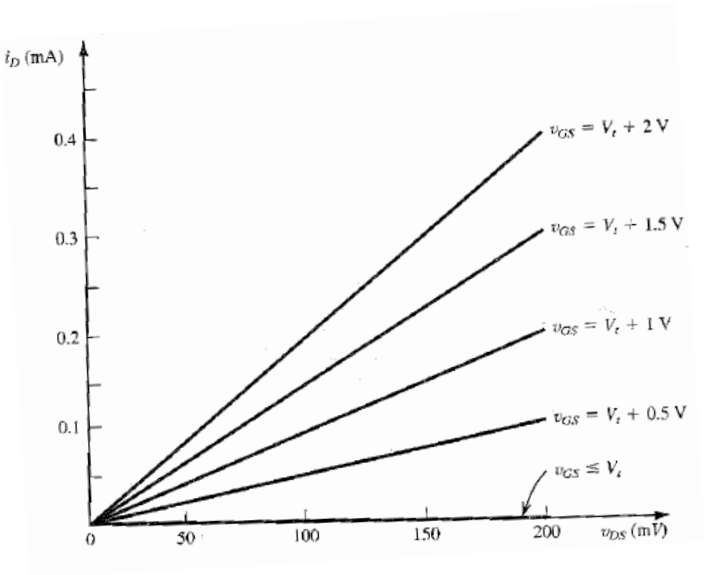


Fig.3.4: The i_D - v_{DS}characteristics of MOSFET in Fig.4.3 when the voltage applied between drain and source, $v_{DS}$is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

- Figure 3.4 shows a sketch of $i_D$versus $v_{DS}$for various values of v_{GS}. We observe that theMOSFET is operating as a **linear resistance** whose value is controlled by v_{GS}. The resistanceis infinite for $v_{GS}<V_t$, and its value decreases as v_{GS}exceeds V_t.
- ***Conclusion:*** For the MOSFET to conduct, a channel has to beinduced. Then, increasing v_{GS}above the threshold voltage V_t, enhances the channel, hencethe names **enhancement-mode operation** and **enhancement-type MOSFET.** Finally,we note that the current that leaves the source terminal (i_S) is equal to the current that enter the drain terminal (i_D), and the gate current $i_G = 0$.

3.1.5 Operation as $v_{DS}$is increased

- If v_{DS} is increased, $v_{GS}$is to be held constant at a value greater than V_t. Referring to Fig. 3.5, and v_{DS}appears as a voltage drop across the length of the channel. That is, as we travel along

the channel from source to drain, the voltage (measured relative to the source) increases from 0 to v_{DS}.

- Thus the voltage between the gate and points along the channel decreases from v_{GS}at the source end to (v_{GS} - v_{DS})at the drain end.
- Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather, the channel will take the tapered form shown in Fig. 3.5, being deepest at the source end and shallowest at the drain end.
- As $v_{DS}$is increased, the channel becomes more tapered and its resistance increases correspondingly.
- Thus the i_D-v_{DS}curve does not continue as a straight line but bends as shown in Fig. 3.6.
- Eventually, when $v_{DS}$is increased to the value that reduces the voltage between gate and channel at the drain end to V_t - that is,

$$v_{GD} = V_t \qquad \text{or} \qquad (v_{GS} - v_{DS}) = V_t \qquad \text{or} \qquad v_{DS} = v_{GS} - V_t$$

the channeldepth at the drain end decreases to almost zero, and the channel is said to be pinched off.

- Increasing v_{DS} beyond this value has little effect on the channel shape, and the current through the channel remains constant at the value reached for $v_{DS} = (v_{GS} - V_t)$.
- The drain current thus saturates at this value, and the MOSFET is said to have entered the saturation region of operation. The voltage v_{DS} at which saturation occurs is denoted v_{DS}(sat).

$$V_{DS}(sat) = (V_{GS} - V_t) \qquad (3.1)$$

- Obviously, for every value of $v_{GS} > V_t$,there is a corresponding value of $v_{DS}(sat)$.The device operates in the saturation region if $v_{DS} > v_{DS}(sat)$.
- The region of the i_D-v_{DS}characteristic obtained for $v_{DS} < v_{DS}(sat)$is called the **triode region.**

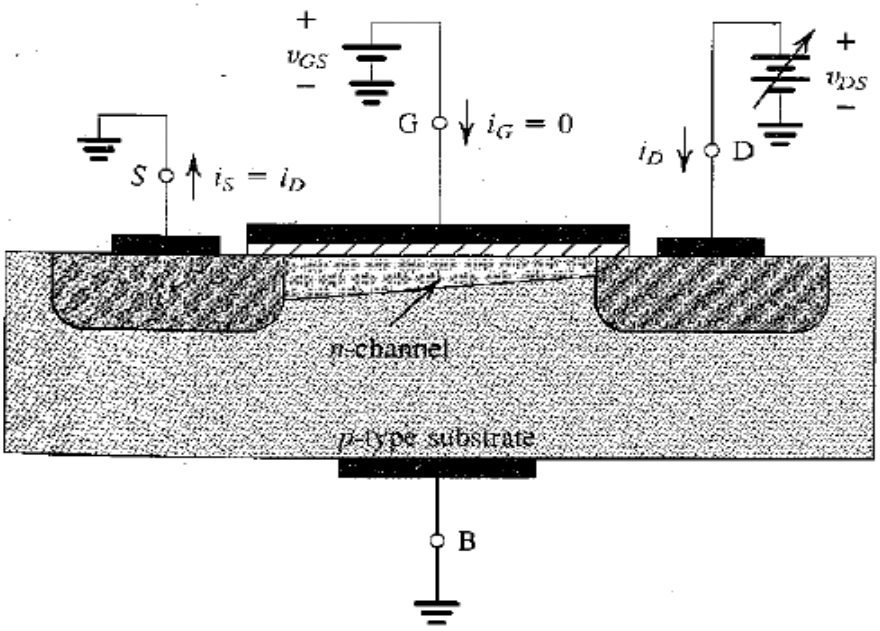


Fig.3.5: Operation of the enhancement NMOS transistor as $V_{DS}$is increased. The induced channelacquires a tapered shape, and its resistance increases as $V_{DS}$is increased. Here, $V_{GS}$is kept constant at avalue > Vt.

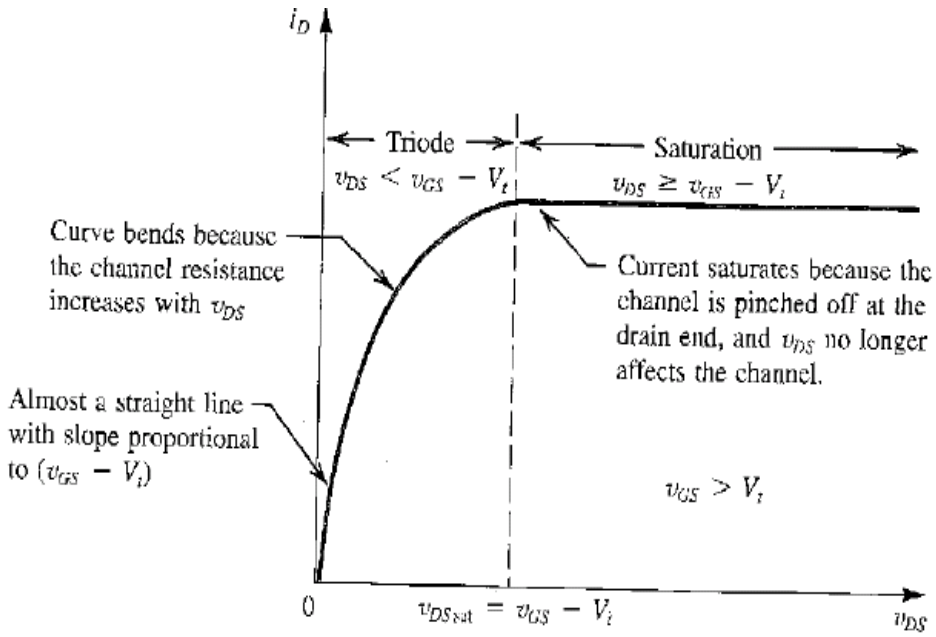


Fig.3.6:The drain current $i_D$versus the drain-to-source voltage $v_{DS}$for an enhancement-type NMOStransistor operated with $v_{GS}>V_t$.

- To visualize the effect of v_{DS}, consider Fig. 3.7 in which channel is modified as $v_{DS}$is increased while $v_{GS}$is kept constant.

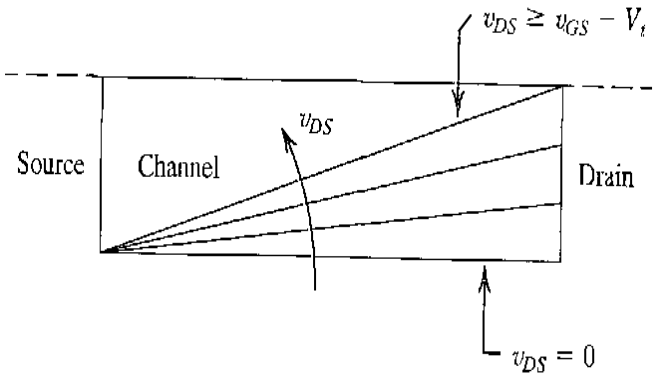


Fig.3.7: Increasing v_{DS}causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches (v_{GS} - V_t), the channel is pinched off at the drain end. Increasing v_{DS}above (v_{GS} - V_t), has little effect on the channel's shape.

- Theoretically, any increase in v_{DS}above$V_{DS}(sat)$ which is equal to (v_{GS} - V_t),has no effect on the channel shape and simply appears across the depletion region surrounding the channel and the n^+ drain region.

3.1.6 Derivation of the i_D- v_{DS}relationship

- Assume that a voltage $v_{GS}$is applied between gate and source with $v_{GS}>Vt$to induce a channel. Also, assume that a voltage $v_{DS}$is applied between drain and source.
- Consider operation in the triode region, for which the channel must be continuous and thus v_{GD}must be greater than $V_t$or, equivalently, $v_{DS}<(v_{GS} - V_t)$. In this case the channel will have the tapered shape shown in Fig.3.8.

- We know that in the MOSFET, the gate and the channel region form a parallel platecapacitor for which the oxide layer serves as a dielectric. If the capacitance per unitgate area is denoted C_{ox} and the thickness of the oxide layer is t_{ox}, then

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (3.2)$$

Where, $\varepsilon_{ox}$is the permittivity of the silicon oxide,

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

The oxide thickness $t_{ox}$is determined by the process technology used to fabricate theMOSFET.

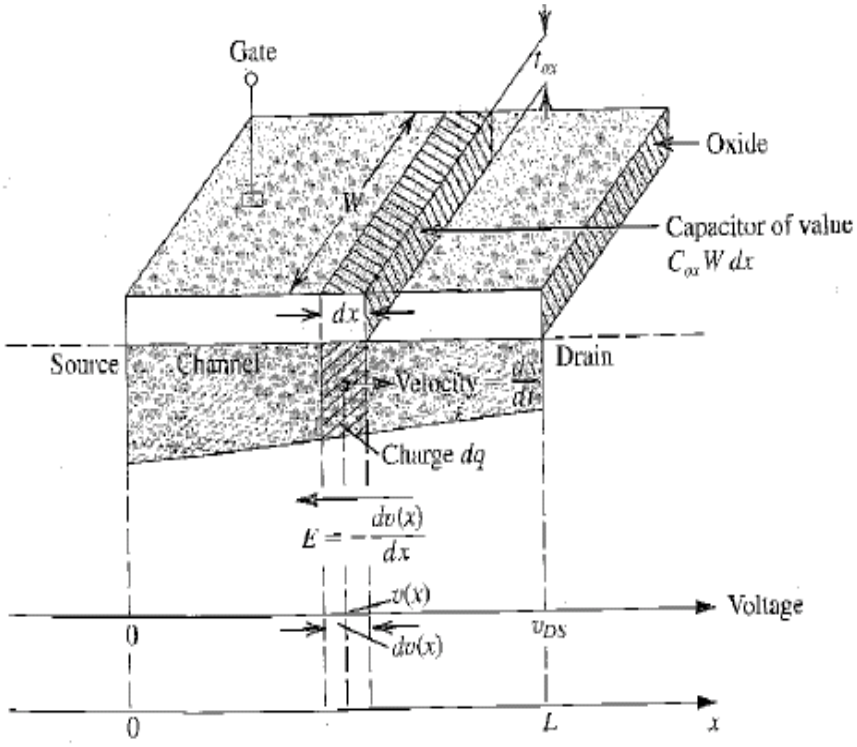


Fig.3.8: Derivation of the $i_D - v_{DS}$characteristic of the NMOS transistor.

- Consider the infinitesimal strip of the gate at distance *x* from the source.
- The capacitance of this strip is $C.\varepsilon_{OX}.W.dx$.
- To find the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the *effective voltage* between the gate and the channel at point *x*

- Where the effective voltage is the voltage that is responsible for inducing the channel at point *x* and is thus $[v_{GS}- v(x) - V_t]$ where $v(x)$ is the voltage in the channel at point *x.* It follows that the electron charge *dq*in the infinitesimalportion of the channel at point *x* is

$$dq = - C_{ox} (W\, dx\,) [\, v_{GS} - v(x) - V_t] \qquad (3.3)$$

where, the leading negative sign accounts for the fact that dqis a negative charge.

- The voltage v_{DS} produces an electric field along the channel in the negative x direction.At point *x*this field can be expressed as

$$E(x) = -\frac{dv(x)}{dx}$$

The electric field $E(x)$ causes the electron charge *dq*to *drift* toward the drain with a velocity, *dx/dt*

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx} \qquad (3.4)$$

Where, $\mu_n$is the mobility of electrons in the channel (called surface mobility).It is a physicalparameter whose value depends on the fabrication process technology.

- The resulting drift current *i* can be obtained as follows:

$$i = \frac{dq}{dt}$$
$$= \frac{dq}{dx}\frac{dx}{dt}$$

- Substituting for the charge-per-unit-length *dq/dx* from Eq. (3.3), and for the electron drift Velocity, *dx/dt*from Eq. (3.4), results in

$$i = -\mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

At a particular point in the channel, the current *i* must be constant at all points along the channel.Thus,*i* must be equal to the source-to-drain current.

$$i_D = -i = \mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

which can be rearranged in the form

$$i_D\,dx = \mu_n C_{ox} W [v_{GS} - V_t - v(x)]\,dv(x)$$

Integrating both sides of this equation from $x = 0$ to $x = L$ and, correspondingly, for $v(0) = 0$to $v(L) = V_{DS}$,

$$\int_0^L i_D\,dx = \int_0^{v_{DS}} \mu_n C_{ox} W [v_{GS} - V_t - v(x)]\,dv(x)$$

gives

$$i_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad (3.5)$$

This is the expression for the i_D-v_{DS}characteristic in the triode region.

- The value of the current at the edge of the triode region or, equivalently, at the beginning of the saturation region can be obtained bysubstituting $v_{DS} = (v_{GS} - V_t)$resulting in

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad (3.6)$$

This is the expression for the i_D-v_{DS}characteristic in the saturation region.

- It givesthe saturation value of $i_D$corresponding to the given v_{GS}(we know that in saturation $i_D$remains constant for a given v_{GS}as $v_{DS}$is varied).
- In the expressions in Eqs. (3.5) and (3.6), $\mu_n C_{ox}$is a constant determined bythe process technology used to fabricate the n-channel MOSFET. It is known as the **process transconductance parameter.**
- It determines the value of the MOSFET transconductance, is denoted k_n', and has the dimensions of A/V^2:

$$K_n' = \mu_n C_{ox} \qquad (3.7)$$

- The i_D-v_{DS}expressions in Eqs. (3.5) and (3.6) can be written in terms of k_n' asfollows:

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{(Triode region)}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \quad \text{(Saturation region)}$$

Where ($\mu_n C_{0X}$) and k_n 'can be interchangeable.

- From Eqs. (3.5) and (3.6) we can see that the drain current is proportional to the ratio of the channel width *W* to the channel length *L*, known as the **aspect ratio** of the MOSFET. Thevalues of *W* and *L* can be selected by the circuit designer to obtain the desired *i-v* characteristics.

3.1.7 The p-Channel MOSFET

- A p-channel enhancement-type MOSFET (PMOS transistor), fabricated on an n-type substratewith p^+regions for the drain and source, has holes as charge carriers.
- The device operates in the same manner as the n-channel device except that $v_{GS}$and v_{DS} are negative and thethreshold voltage $V_t$is negative. Also, the current $i_D$enters the source terminal and leavesthrough the drain terminal.
- PMOS technology originally dominated MOS manufacturing. Because NMOSdevices can be made smaller and thus operate faster, and because NMOS historically requiredlower supply voltages than PMOS, NMOS technology has virtually replaced PMOS.
- PMOS transistor is most familiar for two reasons: a) PMOS devicesare still available for discrete-circuit design, and b) both PMOS and NMOStransistors are utilized in complementary MOS or CMOScircuits, which is currently thedominant MOS technology.

3.2 Current – Voltage characteristics

These characteristics can be measured at dc or at low frequencies and thus are called static characteristics.

3.2.1 Circuit Symbol

- Figure 3.10(a) shows the circuit symbol for the n-channel enhancement-type MOSFET. The spacing between the two vertical lines that represent the gate and the channel indicates the fact that the gate electrode is insulated from the body of the device.The polarity of the p -type substrate (body) and the *n* channel is indicated by the arrowhead on the line representing

the body (B). This arrowhead also indicates the polarity of the transistor, namely, that it is an n-channel device.

- In Fig. 3.10(b), an arrowhead is placed on the source terminal, thus distinguishing it from the drain terminal. The arrowhead points in the normal direction of current flow and thus indicates the polarity of the device (i.e., *n* channel). Observe that in the modified symbol, there is no need to show the arrowhead on the body line.
- The circuit symbol ofFig. 3.10(b) clearly distinguishes the source from the drain, in practice it is the polarity ofthe voltage impressed across the device that determines source and drain; *the drain is alwayspositive relative to the source in an n-channel FET.*
- In applications where the source is connected to the body of the device, a further simplificationof the circuit symbol is possible, as indicated in Fig. 3.10(c).

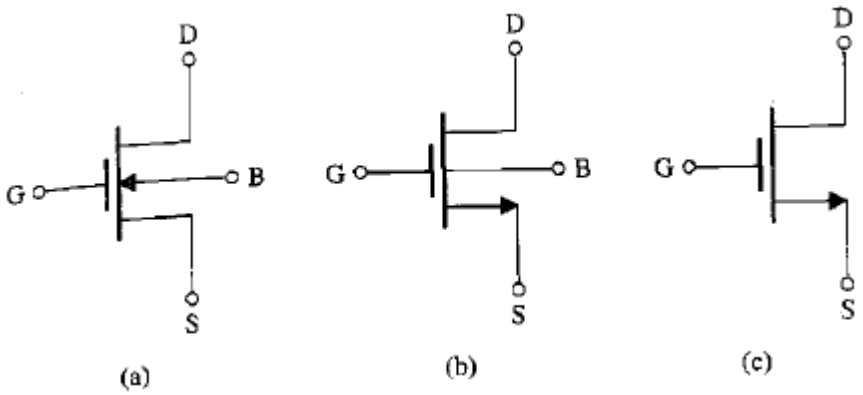


Fig.3.10: (a) Circuit symbol for the w-channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel), (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

3.2.2 The i_D-v_{DS}characteristics

Figure 3.11(a) shows an n-channel enhancement-type MOSFET with voltages $v_{GS}$and v_{DS}applied and with the normal directions of current flow indicated. This circuit canbe used to measure the i_D- v_{DS}characteristics, which are a family of curves, each measuredat a constant v_{GS}.We

expecteach of the i_D- v_{DS}curves to have the shape shown in Fig. 3.6. From Fig. 3.11(b), which shows a typical set of i_D- v_{DS}characteristics.

The characteristic curves in Fig. 3.11(b) indicate that there are three distinct regions ofoperation:

a) the **cutoff region –** FET can be used as an OFF switch
b) the **triode region -** FET can be used as an ON switch
c) the **saturation region -** FET can be used as an amplifier

- The device is **cut off** when $v_{GS}<V_t$.To operate the MOSFETin the **triode region** we must first induce a channel,

$$v_{GS}>V_t \qquad \text{(Induced channel)} \qquad (3.8)$$

and then keep v_{DS} small enough so that the channel remains continuous. This is achieved byensuring that the gate-to-drain voltage is

$$V_{GD}>V_t \qquad \text{(Continuous channel)} \qquad (3.9)$$

This condition can be stated explicitly in terms of v_{DS} by writing

$$v_{GD}= v_{GS}+ v_{SD} = v_{GS}- v_{DS}$$

thus, $(v_{GS}- v_{DS}) >V_t$

which can be rearranged to obtain

$$v_{DS}< (v_{GS}- V_t) \qquad \text{(continuous channel)} \qquad (3.10)$$

- Either Eq. (3.9) or Eq. (3.10) can be used to obtain triode-region operation. In words, *then-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t and the drain voltage is lower than the gate voltage by at least V_t volts.*

- In the triode region, the i_D- v_{DS}characteristics can be described by the relationship of Eq. (3.5), which we repeat here,

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \qquad (3.11)$$

Where, $\mu_n C_{0X} = k_n'$ *is* called the process transconductance parameter; its value is determined bythe fabrication technology.

- If $v_{DS}$is sufficiently small so that we can neglect the v_{DS}^2term in Eq. (3.11), we obtain for the i_D- v_{DS}characteristics near the origin the relationship

$$i_D \approx k_n' \frac{W}{L}(v_{GS} - V_t) v_{DS} \qquad (3.12)$$

This linear relationship represents the operation of the MOS transistor as a linear resistance, r_{DS}whose value is controlled by v_{GS}. Specifically, for v_{GS}set to a value V_{GS}, $r_{DS}$is given by

$$r_{DS} \equiv \left.\frac{v_{DS}}{i_D}\right|_{\substack{v_{DS}\ \text{small} \\ v_{GS} = V_{GS}}} = \left[k_n' \frac{W}{L}(V_{GS} - V_t)\right]^{-1} \qquad (3.13)$$

The r_{DS}can be expressed in terms of the **gate-to-source overdrive voltage,**

$$\mathbf{V_{OV} = V_{GS} - V_t} \qquad (3.14)$$

$$r_{DS} = 1 \Big/ \left[k_n' \left(\frac{W}{L}\right) V_{OV}\right] \qquad (3.15)$$

Eq. (3.12)is based on the assumption that $v_{DS} < 2V_{0V}$.

To operate the MOSFET in the saturation region, a channel must be induced,

$$v_{GS} \geq V_t \quad \text{(Induced channel)} \qquad (3.16)$$

and pinched off at the drain end by raising $v_{DS}$to a value that results in the gate-to-drainvoltage falling below V_t,

$$v_{GD} \leq V_t \quad \text{(Pinched-off channel)} \qquad (3.17)$$

This condition can be expressed explicitly in terms of v_{DS}as

$$v_{DS} \geq v_{GS} - V_t \quad \text{(Pinched-off channel)} \qquad (3.18)$$

In words, *the n-channel enhancement-type MOSFET operates in the saturation region when*

v_{GS} is greater than V_t , and the drain voltage does not fall below the gate voltage by more thanV_t volts.

- The boundary between the triode region and the saturation region is characterized by

$$v_{DS} = v_{GS} - V_t \quad \text{(Boundary)} \qquad (3.19)$$

Substituting this value of v_{DS}into Eq. (3.11) gives the saturation value of the current $i_D$as

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 \qquad (3.20)$$

- Thus **in saturation the MOSFET provides a drain current whose value is independent of thedrain voltage $v_{DS}$and is determined by the gate voltage v_{GS}**according to the square-law relationshipin Eq. (3.20), a sketch of which is shown in Fig. 3.12.
- Since the drain currentis independent of the drain voltage, the saturated **MOSFET behaves as an ideal currentsource** whose value is controlled by v_{GS}according to the nonlinear relationship in Eq. (3.20).
- Figure 3.13 shows a circuit representation of this view of MOSFET operation in the saturation region. This is a **large-signal equivalent-circuit model.**
- Since $v_{DS} = v_{GS} - V_t$, either in triode region or in saturation region drain current is given by

$$i_D = \frac{1}{2} k_n' \frac{W}{L} v_{DS}^2 \qquad (3.21)$$

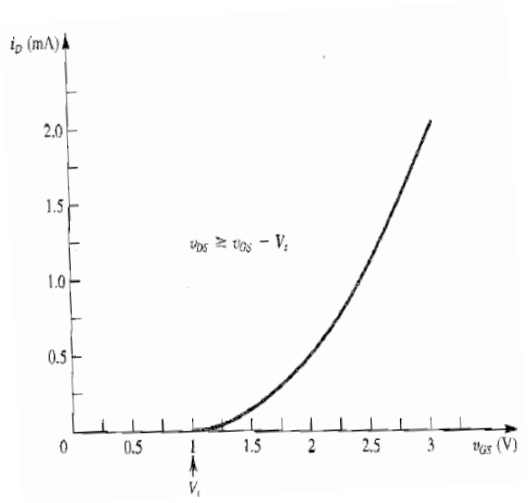


Fig.3.11: The i_D- v_{DS} characteristic for an enhancement type NMOS transistor in saturation.

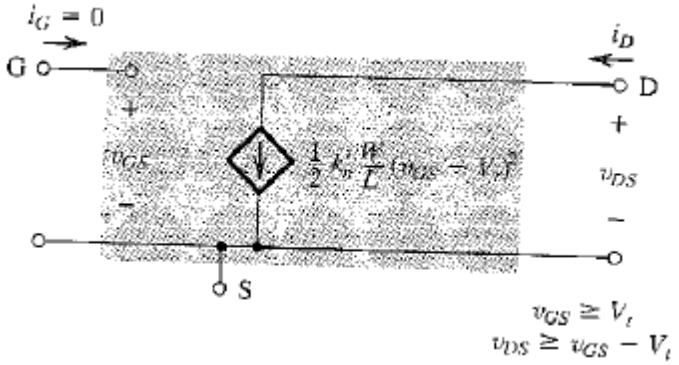


Fig. 3.12: Large-signal equivalent-circuit model of an n-channel MOSFET operating in the saturation region.

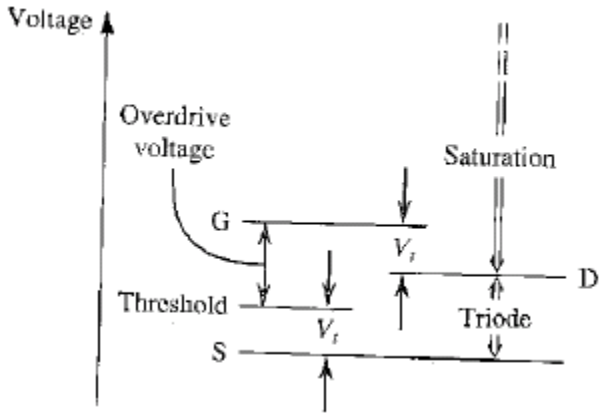


Fig. 3.13: The relative levels of theterminal voltages of the enhancement NMOStransistor for operation in the triode region andin the saturation region.

3.2.3 Finite Output Resistance in Saturation

- Equation (3.12) and the corresponding large-signal equivalent circuit in Fig. 3.13 indicatethat in saturation, $i_D$is independent of $v_{DS.}$
- Thus a change Δv_{DS}in the drain-to-source voltagecauses a zero change in i_D, which implies that the incremental resistance looking intothe drain o f a saturated MOSFET is infinite.
- Once the channel is pinched off at the drain end, further increases in v_{DS}have noeffect on the channel's shape.
- But in practice as $v_{DS}$is increased, the channel pinch-off point is moved slightlyaway from the drain, toward the source. This is illustrated in Fig. 3.15, from which we can observe that the voltage across the channel remains constant at v_{GS} -V_t= v_{DS}*(sat)*and the additionalvoltage applied to the drain appears as a voltage drop across the narrow depletion regionbetween the end of the channel and the drain region.
- This voltage accelerates the electronsthat reach the drain end of the channel and sweeps them across the depletion region into thedrain. That (with depletion—layer widening) the channel length is in effectreduced, from L to $L - \Delta L$,a phenomenon known as **channel-length modulation**.
- Since $i_D$is inversely proportional to the channel length (Eq. 3.20), $i_D$increases with $v_{DS.}$

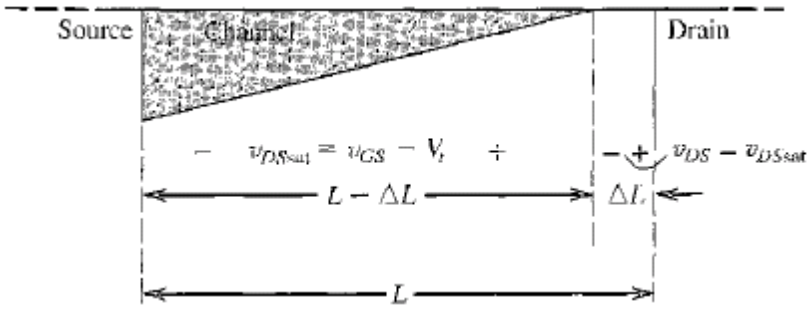


Fig.3.14:Increasing v_{DS}beyond v_{DS} *(sat)* causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

- To account for the dependence of $i_D$on v_{DS}in saturation, we replace L in Eq. (3.20) with

L - ΔL to obtain

$$i_D = \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2$$
$$= \frac{1}{2}k_n'\frac{W}{L}\frac{1}{1-(\Delta L/L)}(v_{GS}-V_t)^2$$
$$\cong \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)(v_{GS}-V_t)^2$$

Assuming that (ΔL/L) << 1 and ΔLis proportional to v_{DS}, ΔL = $\lambda' v_{DS}$

where, λ' is a process-technology parameter with the dimensions of μm/V, we get

$$i_D = \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\lambda'}{L}v_{DS}\right)(v_{GS}-V_t)^2$$

$$\lambda = \frac{\lambda'}{L}$$

It follows that λ is a process-technology parameter with the dimensions of V^{-1} and that, fora given process;λ is inversely proportional to the length selected for the channel. In termsof λ, the expression for i_D becomes

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) \qquad (3.22)$$

- A typical set of i_D-v_{DS}characteristics showing the effect of channel-length modulation isdisplayed in Fig. 3.16.
- The observed linear dependence of $i_D$on v_{DS}in the saturation region is represented in Eq. (3.22) by the factor (1 + λ v_{DS}).
- From Fig. 3.16 we observe that when the straight-line i_D-v_{DS} characteristics are extrapolated they intercept the v_{DS} -axis at the point v_{DS} = -V_A, where $V_A$is a positive voltage.
- Equation (3.22), however, indicates that i_D = 0 at v_{DS} = - 1 / λ. It follows that V_A= 1/ λ

$$V_A = V_A'L$$

Where, V_A' is a process-technology parameter with the dimensions of V/μm.

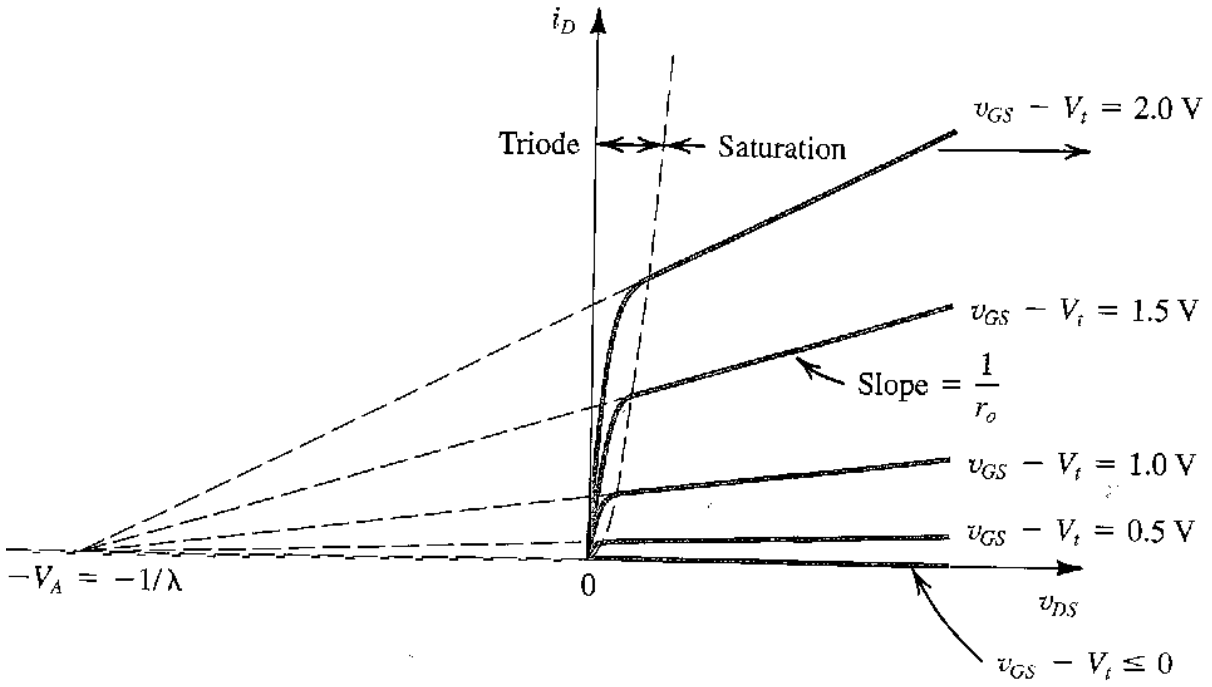


Fig. 3.15: Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

- Equation (3.22) indicates that when channel-length modulation is taken into account, the saturation values of i_D depend on v_{DS}.
- Thus, for a given v_{GS}, a change Δv_{DS} yields a corresponding change Δi_D in the drain current i_D.
- It follows that the output resistance of the current source representing i_D in saturation is no longer infinite. Defining the output resistance r_O as

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}} \tag{3.23}$$

And using Eq. (3.22) results in

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1} \tag{3.24}$$

which can be written as

$$r_o = \frac{1}{\lambda I_D} \tag{3.25}$$

$$r_o = \frac{V_A}{I_D} \tag{3.26}$$

or equivalently

where, I_D is the drain current with-out channel-length modulation taken into account.

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

Thus the output resistance is inversely proportional to the drain current.

- Fig. 3.16 shows the large-signal equivalent circuit model incorporating r_O.

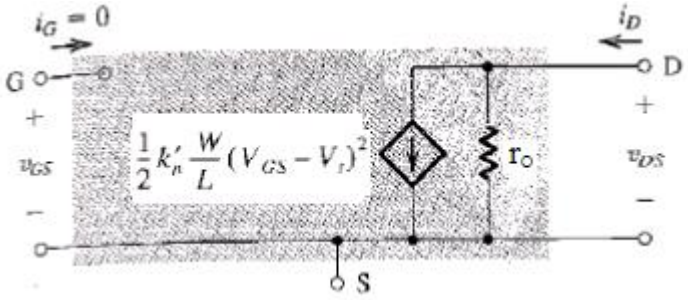


Fig. 3.16: Large-signal equivalent circuit model of the n-channel MOSFET in saturation, incorporating the output resistance r_0. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq.(3.22)

3.2.4 Characteristics of the p-Channel MOSFET

- The circuit symbol for the p-channel enhancement-type MOSFET is shown in Fig. 3.17(a).
- Figure 3.17(b) shows a modified circuit symbol in which an arrowhead pointing in the normaldirection of current flow is included on the source terminal.
- For the case where thesource is connected to the substrate, the simplified symbol of Fig. 3.17(c) is usually used.
- The voltage and current polarities for normal operation are indicated in Fig. 3.17(d). Recallthat for the p-channel device the threshold voltage V_t **is negative**.
- To induce a channel weapply a gate voltage that is more negative than V_t,

$$v_{GS} \leq V_t \text{(Induced channel)} \quad \text{(or) equivalently } v_{SG} \geq |V_t| \tag{3.27}$$

and apply a drain voltage that is more negative than the source voltage (i.e., v_{DS} is negativeor, equivalently, v_{SD} is positive). The current i_D flows out of the drain terminal, as indicatedin the figure.

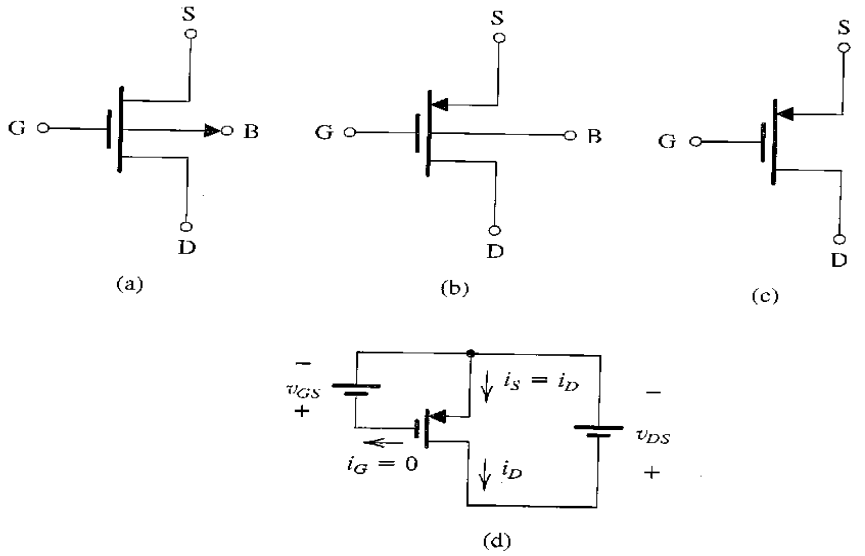


Fig.3.17: (a) Circuit symbol for the p-channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead, (c) Simplified circuit symbol for the case where the source is connected to the body, (d) The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

- To operate in the triode region v_{DS} must satisfy

$$v_{DS} \geq (v_{GS} - V_t) \qquad \text{(Continuous channel)} \qquad (3.28)$$

  i.e., the drain voltage must be higher than the gate voltage by at least $|V_t|$.

- The current i_D is given by the same equation as for NMOS, Eq. (3.11), except for replacing k'_n with k'_p,

$$i_D = k'_p \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad (3.29)$$

Where, v_{DS}, v_{GS} *and* $V_t$are negative and the transconductance parameter $k'_p$is given by

$$k_p' = \mu_p C_{ox} \tag{3.30}$$

Where, μ_p is the mobility of holes in the induced p-channel. Typically, μ_p = 0.25 to 0.5 μ_n andis process-technology dependent.

- To operate in saturation, v_{DS} must satisfy the relationship

$$v_{DS} \leq (v_{GS} - V_t) \qquad \text{(Pinched-off channel)} \tag{3.31}$$

- The current $i_D$is given by the same equation used for NMOS, Eq. (4.22), again with k'$_n$ replaced with k'$_p$,

$$i_D = \frac{1}{2} k_p' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \tag{3.32}$$

Where, v_{DS}, v_{GS}, λ *and* $V_t$are negative

- To turn a PMOS transistor on, the gate voltage has to be made lower than thatof the source by at least | V_t| to operate in the triode region, the drain voltage has to exceed that of the gate by at least | V_t|,otherwise, the PMOS operates in saturation.
- The chart in Fig. 3.18 provides a pictorial representation of these operatingconditions.

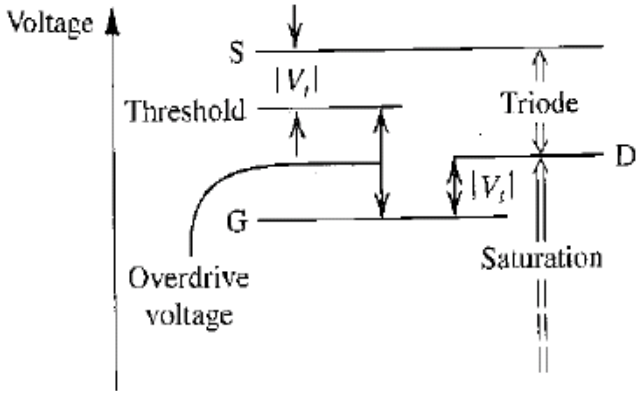


Fig.3.18: The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

3.2.5 The Role of the Substrate-The Body Effect

- In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the p-n junction between the substrate and the induced channel (see Fig. 3.5)having a constant zero (cutoff) bias.
- In such a case the substrate does not play any role in the circuit operation and its existence can be ignored altogether.
- In integrated circuits, however, the substrate is usually common to many MOS transistors.
- In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the mostpositive in a PMOS circuit).
- The resulting reverse-bias voltage between source and body(V_{SB} in an n-channel device) will have an effect on device operation.
- To appreciate this fact, consider an NMOS transistor and let its substrate be made negative relative to the source. The reverse bias voltage will widen the depletion region (refer to Fig. 3.2).
- This in turnreduces the channel depth. To return the channel to its former state, V_{GS} has to be increased.
- The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_t. Specifically, it has been shown that increasing the reverse substratebias voltage V_{SB} results in an increase in V_t, according to the relationship

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \qquad (3.33)$$

Where,$V_{t0}$is the threshold voltage for V_{SB}= 0 and $\Phi_f$is a physical parameter with ($2\Phi_f$) = 0.6V; $\gamma$is a fabrication-process parameter and is given by

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}} \qquad (3.34)$$

Where, q is the electron charge and N_A is doping concentration of p-type substrate and $\varepsilon_r$is the relative permittivity of silicon (11.7 ε_0= 11.7 x 8.857x10^{-14} = 1.04 x 10^{-12} F/cm). The parameter γhas the dimensions of $\sqrt{V}$ = 0.4 $V^{1/2}$.

- For p-channel devices with v_{SB} replaced by the reverse bias of the substrate, v_{BS} (or, alternatively, replace v_{SB} by $|v_{SB}|$) and note that is negative. Inevaluatingγ, N_A must be replaced with N_D, the doping concentration of the n well inwhich the PMOS is formed. Forp-channel devices, $2\Phi_f$= 0.75 V, and γ is typically- 0.5$V^{1/2}$.
- Equation (3.33) indicates that an incremental change in v_{SB} gives rise to an incremental change in V_t, which in turn results in an incremental change in i_D even though v_{GS} mighthave been kept constant.
- It follows that the body voltage controls i_D; thus the body acts as another gate for the MOSFET, a phenomenon known as the **body effect**. Here we note that the parameter γ is known as the body-effect parameter.

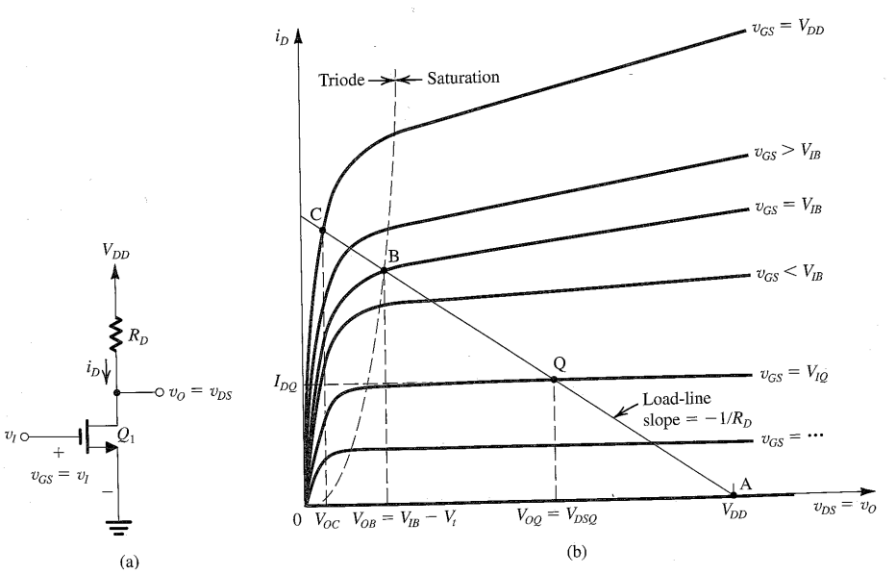
3.4 MOSFET as an amplifier and as a switch

- The MOSFET is used in the design of amplifier circuits. When it is operated in the saturation region, acts as a voltage-controlled current source: Changes in the gate-to-source voltage, v_{GS}gives rise to changes in the drain currenti_D.Thus the saturated MOSFET can be used as a transconductance amplifier.
- Since for linear amplification (in amplifiers whose output signal is linearly related to their input signal) it is necessary to obtain linear amplification from a fundamentally nonlinear device is dc biasing the MOSFET to operate at a certain appropriate V_{GS} and a corresponding I_D and then superimposing the voltage signal to be amplified, v_{gs} on the dc bias voltage V_{GS}. By keeping v_{gs} a small value, the resulting change in drain current id can be made proportional to v_{gs}.
- **Large signal operation:** From the voltage transfer characteristics it is observed the region over which the transistor can be biased to operate as a small-signal amplifier as

well as the region where it can be operated as a switch. MOS switches find application in both analog and digital circuits.

3.4.1 Large-signal operation- The transfer characteristics

- The basic structure of the most commonly used MOSFET amplifier, the common-source (CS) circuit or grounded-source circuit is shown in fig. 3.24 (a).



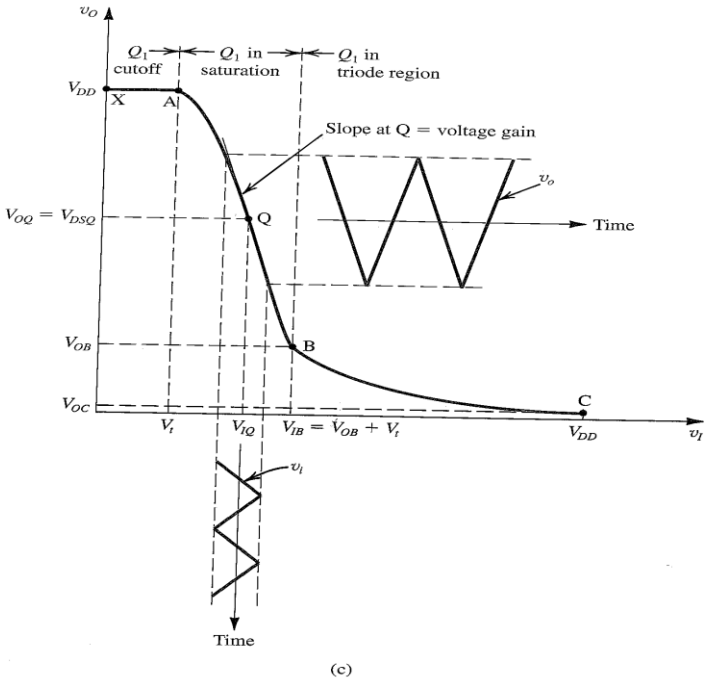


Fig. 3.24: (a) Basic structure of common-source amplifier, (b) Graphical construction to determine the transfer characteristics of CS amplifier, (c) Transfer characteristics showing operation as an amplifier biased at point Q

- The circuit is viewd as a two-port network, since the grounded source terminal is common to both the input port, between gate and source, and the output port between drain and source. The basic control action of MOSFET is that changes in v_{GS}give rise to changes in i_D, we are using a resistor R_D to obtain an output voltage v_0,

$$v_0 = v_{DS} = V_{DD} - R_D i_D \qquad (3.35)$$

- In this way transconductance amplifier is converted into voltage amplifier.
- **Voltage transfer characteristics:** These are the plots between the output voltage for various values of input voltage. The transfer characteristics are obtained in two ways: graphically and analytically.

3.4.2. Graphical derivation of the Transfer Characteristics

- The operation of the common-source circuit is governed by the MOSFET's i_D-v_{DS} characteristics and by the relation between i_D and v_{DS} imposed by connecting the drain to the power supply V_{DD} via resistor R_D

$$v_{DS} = V_{DD} - R_D i_D \qquad (3.36)$$

or, equivalently,

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \qquad (3.37)$$

- Figure 3.24 (b) shows the i_D-v_{DS}characteristic curves superimposed on which is a straight line representing the i_D-v_{DS}relationship of Eq. (3.37).
- It is observed that the straight line intersects the v_{DS}-axis at V_{DD} and has a slope of -1/R_D. Since R_D is load resistor of the amplifier. The straight line in the Fig. 3.24(b) is known as the **load line**.
- The graphical construction of Fig. 3.24(b) is used to determine v_0 (equal to v_{DS}) for each given value of v_I (v_{GS} = vI). For a given value of v_I, we locate the corresponding i_D-v_{DS} curve and find $v0$ from the point of intersection of this curve with the load line.

$$V_{OB} = V_{IB} - V_t$$

- For $v_I > V_{IB}$, the transistor is driven deeper into the triode region. Because of the characteristics curves in the triode region are bunched together, the output voltage decreases slowly towards zero.
- At a particular operating point C obtained for $v_I - V_{DD}$, the corresponding output voltage V_{0C} will be very small. This point by point determination of the transfer characteristic results in the transfer curve shown in Fig. 3.24(c).
- It is observed three distinct segments, each corresponding to one of the three regions of operation of MOSFET Q_1

3.4.3 Operation as a switch

- When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve.
- The device is turned off by keeping $v_I < V_t$ resulting in operation some where on the segment XA with $v_0 - V_{DD}$.
- The switch is turned on by applying a voltage close to V_{DD}, resulting in operation close to point C with v_0 very small (at C, $v_0 = V_{0C}$)
- The common source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0V and the "hign" level close to V_{DD}.

3.4.4 Operation as a Linear Amplifier

- To operate the MOSFET as an amplifier it should be in the saturation mode segment of the transfer curve.
- The device is biased at a point close to the middle of the curve; point Q is a good example of an appropriate bias point. It is also called as **quiescent point**.
- The voltage signal to be amplified *vi* is then superimposed on the dc voltage V_{IQ} as shown in Fig.3.24(c)
- The value of v_i is sufficiently small to operate in linear segment of the transfer curve, the resulting output voltage signal v_0 will be proportional to v_i i.e., the amplifier will be very nearly linear, and v_0 will have the same waveform as vi except it will be larger by a factor equal to voltage gain (A_v) of the amplifier at Q. Where,

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}} \qquad (3.38)$$

- Thus the voltage gain is equal to the slope of the transfer curve at the bias point Q. It is observed that the slope is negative, and thus the CS amplifier is inverting. This is also shown in Fig. 3.24(c)

3.4.5 Analytical expression for the Transfer Characteristics

- The *i-v* relationships that describes the MOSFET operation in the three regions – cutoff, saturation, and triode – can be easily used to derive analytical expressions for the three segments of the transfer characteristics in Fig. 3.24(a).

The Cutoff-region segment, XA: Here, $v_I \leq V_t$ and $v_0 = V_{DD}$

The Saturation-Region Segment, AQB: Here, $v_I \geq V_t$, $v_0 \geq v_I - V_t$. Neglecting the channel length modulation and substituting for i_D from

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_I - V_t)^2$$

into

$$v_O = V_{DD} - R_D i_D$$

gives

$$v_O = V_{DD} - \frac{1}{2}R_D \mu_n C_{ox}\frac{W}{L}(v_I - V_t)^2 \qquad (3.39)$$

- Incremental voltage gain A_v at a bias point Q at which $v_I = V_{IQ}$ is,

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}}$$

Thus,

$$A_v = -R_D \mu_n C_{ox}\frac{W}{L}(V_{IQ} - V_t) \qquad (3.40)$$

- It is observed that the voltage gain is proportional to the values of R_D, the transconductance parameter $k_n' = \mu_n C_{ox}$, the transistor aspect ratio W/L, and the overdrive voltage at the bias point $V_{OV} = V_{IQ} - V_t$
- Another expression for the voltage gain can be obtained by substituting $v_I = V_{IQ}$ in Eq. (3.39), using Eq. (3.40), and substituting $V_{IQ} - V_t = V_{OV}$. This results,

$$A_v = -\frac{2(V_{DD} - V_{OQ})}{V_{OV}} = -\frac{2V_{RD}}{V_{OV}} \qquad (3.41)$$

Where, V_{RD} is the dc voltage drop across the drain resistor R_D;

i.e., $V_{RD} = V_{DD} - V_{OQ}$

- The end point of the saturation region is characterized by

$$\boldsymbol{V_{OB} = V_{IB} - V_t} \qquad (3.42)$$

- Thus, its coordinates can be determined by substituting $v_O = V_{OB}$ and $v_I = V_{IB}$ in Eq. (3.39) and solving the resulting equation simultaneously with Eq. (3.42)

The Triode-Region Segment, BC: Here, $v_I \geq V_t$ and $v_O \leq v_I - V_t$. Substituting for i_D by the triode-region expression

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right]$$

into

$$v_O = V_{DD} - R_D i_D$$

gives

$$v_O = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right]$$

- The portion of the segment for which v_O is small is given approximately by

$$v_O \cong V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)v_O$$

which reduces to

$$v_O = V_{DD} \Big/ \left[1 + R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)\right] \qquad (3.43)$$

- We can use the expression for r_{DS}, the drain-to-source resistance near the origin of the i_D-v_{DS} plane (Eq. 3.13),

$$r_{DS} = 1 \Big/ \left[\mu_n C_{ox} \frac{W}{L}(v_I - V_t)\right]$$

- Together with Eq. (3.43) to obtain

$$v_O = V_{DD} \frac{r_{DS}}{r_{DS} + R_D} \qquad (3.44)$$

- For small v_0, the MOSFET operates as a resistance r_{DS}, which forms with R_D a voltage divider across V_{DD}. Usually, $r_{DS} << R_D$, and Eq. (3.44) reduces to

$$v_O \cong V_{DD}\frac{r_{DS}}{R_D} \tag{3.45}$$

UNIT – IV

BIPOLAR JUNCTION TRANSISTORS

Objectives: To familiarize with the structure and various characteristic parameters of BJT & its functioning as a switch and amplifier.

Syllabus: Device structure and physical operation, Current-voltage characteristics, BJT as an amplifier and as a switch.

Outcomes:

Students will be able to

- understand the physical structure and operation of BJT circuits.
- calculate BJT parameters from its characteristics.
- understand with the BJT behavior as a switch and amplifier.

4.1 Device structure and physical operation

4.1.1 Simplified structure and modes of operation

- The BJT consists of three semiconductor regions emitter region, base region, collector region.
- There are two types of transistors
  - PNP (collector-p type, emitter- p type, base –n type)
  - NPN (collector-n type, emitter- n type, base- p type)

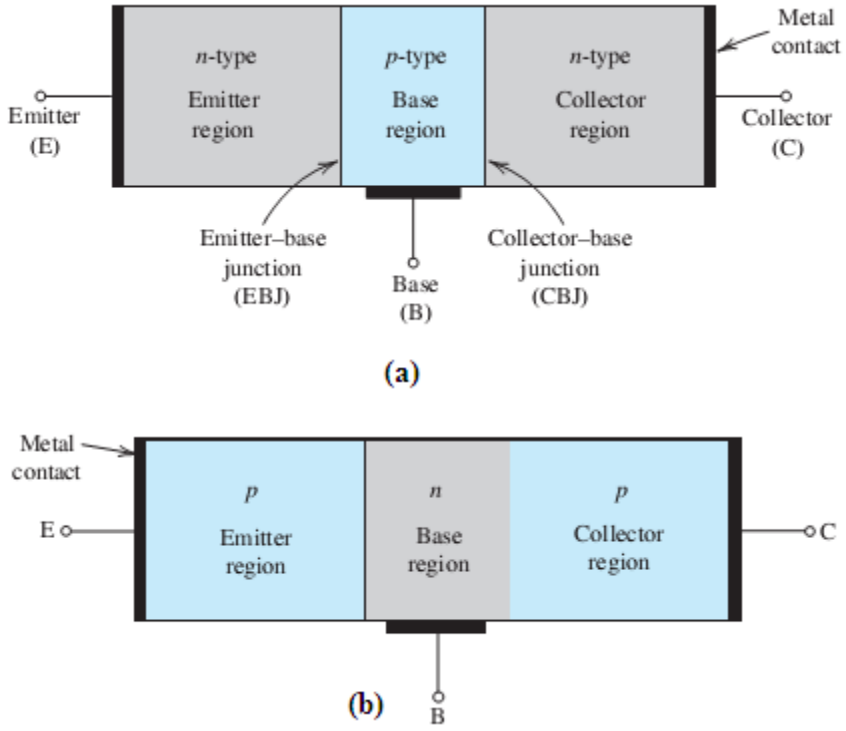


Fig. 4.1: A simplified structure of (a) the *npn* transistor; (b) the *pnp* transistor

- The transistor can be operated in three regions depending on the bias condition
- **The active mode** is forward active mode which is used as an amplifier.
- **The cut off and saturation mode** are called reverse active (or inverse active) used for switching purpose.

Table 4.1: BJT modes of operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

4.1.2 Operation of the npn transistor in active mode

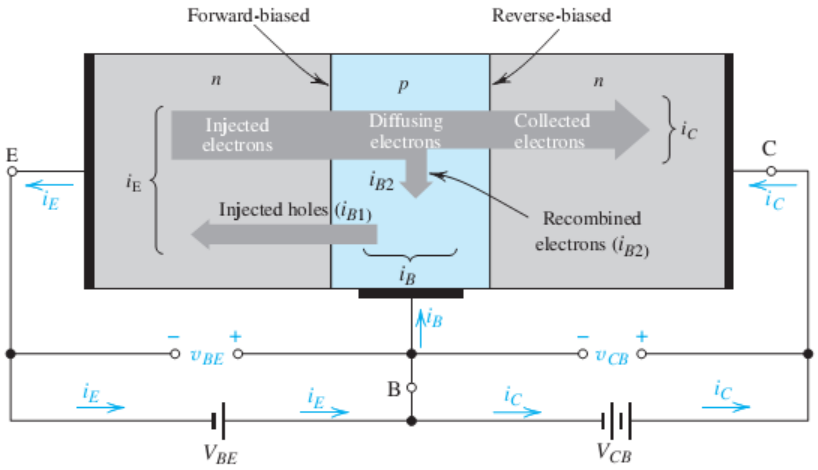


Fig. 4.2: Current flow in an *npn* transistor biased to operate in the active mode

- In active mode operation the emitter to base junction is made forward biased and collector to base junction is reverse biased.
- The current is mainly due to diffusion current components and the drift of minority charge carrier currents are neglected. The current that flows across the emitter – base junction will constitute the emitter current i_E. The direction of i_E is out of the emitter lead, which is in the direction of hole current and opposite to the direction of the electron current .the emitter current is mostly dominated by the hole current since electrons are large in number.
- Let us consider the electrons injected from the emitter to base since the base is very thin, the electron concentration will be highest at the emitter side and lowest at collector side as in the case of any forward biased pn junction the concentration $n_p(0)$ will be proportional to

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \quad \text{.... (4.1)}$$

Where, n_{p0} is thermal equilibrium of minority electron concentration in base region

υ_{BE} is base to emitter voltage

V_T is thermal voltage (=25mv)

$$I_n = A_E q D_n \frac{dn_p(x)}{dx}$$
$$= A_E q D_n \left(-\frac{n_p(0)}{W}\right) \quad \text{.... (4. 2)}$$

Where, A_E = cross-sectional area

Q = charge carriers

Dn = electron diffusion constant

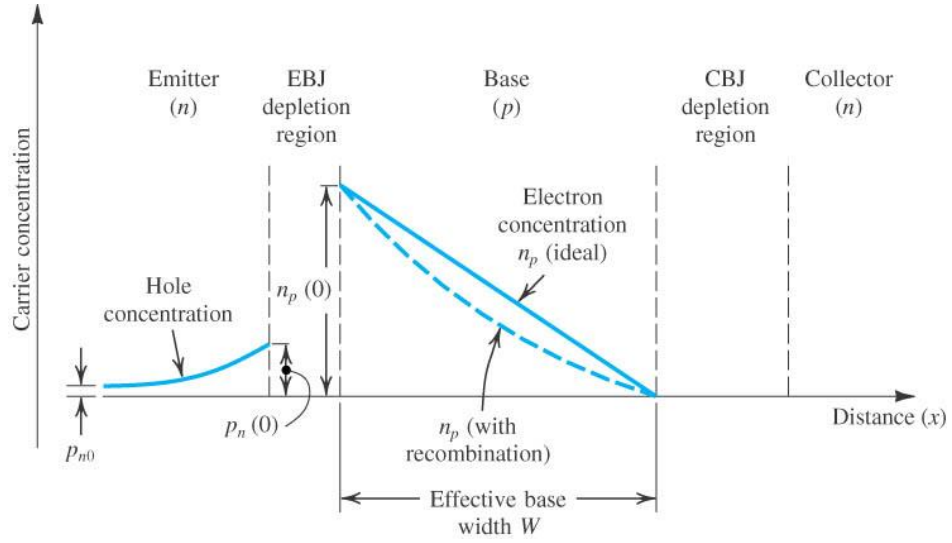


Fig. 4.3: Profiles of minority-carrier concentrations in the base and in the emitter of an *npn* transistor operating in the active mode: $\upsilon_{BE} > 0$ and $\upsilon_{CB} = 0$.

- Some of the electrons diffusing from the base region will combine with holes, which are majority carriers in base. As base is very thin the loss of electrons by this diffusion is very small hence the minority charge carrier current can be very small.

The collector current

- The diffusion electrons reach the collector base region. As the collector is more positive than base the electrons get accumulates across the collector region, then the collector current will be given as

$$i_C = I_S e^{v_{BE}/V_T} \quad \text{.... (4.3)}$$

where the **saturation current** I_S is given by

$$I_S = A_E q D_n n_{p0}/W$$

Substituting $n_{p0} = n_i^2/N_A$, where n_i is the intrinsic carrier density and N_A is the doping concentration in the base, we can express I_S as

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \quad \text{.... (4.4)}$$

- Here the collector current ic does not depends on the collector to base voltage υ_{CB}.
- From the above equation the scaling current is inversely proportional to width of the depletion region and directly proportional to the area of EB junction.
- Typically is in the range of 10^{-12} to 10^{-18} .the scaling current doubles for every 5 degree rise in temperature as it is a function of n_i which is proportional to temperature. The scaling current also varies with respect to area, where for same υ_{BE} voltage the collector current varies for larger device to smaller device.

The Base Current

- The base current is composed of two components .the first current component is due to holes injected from base to emitter region. It is given by

$$i_{B1} = \frac{A_E q D_p n_i^2}{N_D L_p} e^{v_{BE}/V_T} \quad \text{.... (4.5)}$$

Where D_p is diffusion constant

L_p is diffusion length

N_D is doping concentration

- The second component is due to the holes supplied by external circuit to replace the holes lost by recombination process. It is given by the total charge to average life time that a hole combine with electron denoted by τ_b.

Where,

$$i_{B2} = Q_n/\tau_b \qquad (4.6)$$

The minority carrier charge stored In the base region, Q_n can be found by referring Fig.4.4. Q_n is represented by the area of the triangle under the straight-line distribution in the base, thus

$$Q_n = A_E q \times \tfrac{1}{2} n_p(0) W$$

Substituting for $n_p(0)$ from Eq.(4.1) and replacing $n_p(0)$ by n_i^2 / N_A gives

$$Q_n = \frac{A_E q W n_i^2}{2N_A} e^{v_{BE}/V_T} \qquad (4.7)$$

which can be substituted in Eq.(4.6) to obtain

$$i_{B2} = \frac{1}{2}\frac{A_E q W n_i^2}{\tau_b N_A} e^{v_{BE}/V_T} \qquad (4.8)$$

Combining Eqs.(4.5) and (4.8) and utilizing Eq.(4.4), we obtain for the total base current i_B

$$i_B = I_S\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n\tau_b}\right)e^{v_{BE}/V_T} \qquad (4.9)$$

Comparing Eqs. (4.3) and (4.9), we see that i_B can be expressed as a fraction of i_C as follows: $i_B = i_C / \beta \qquad (4.10)$

$$i_B = \left(\frac{I_S}{\beta}\right)e^{v_{BE}/V_T} \qquad (4.11)$$

where β is given by

$$\beta = 1\Big/\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n\tau_b}\right) \qquad (4.12)$$

- Where the beta is transistor constant varies from 50 to 200. For special case diodes it will be 1000 and is called as common emitter current gain.

The emitter current

- The emitter current is given by the sum of base and collector current

$$i_E = i_C + i_B \qquad (4.13)$$

Use of Eqs. (4.10) and (4.13) gives

$$i_E = \frac{\beta+1}{\beta} i_C \qquad (4.14)$$

$$i_E = \frac{\beta+1}{\beta} I_S e^{v_{BE}/V_T} \qquad (4.15)$$

Alternatively, we can express Eq. (4.14) in the form

$$i_C = \alpha i_E \qquad (4.16)$$

where the constant α is related to β by

$$\alpha = \frac{\beta}{\beta+1} \qquad (4.17)$$

Thus the emitter current in Eq. (4.15) can be written

$$i_E = (I_S/\alpha) e^{v_{BE}/V_T} \qquad (4.18)$$

Finally, we can use Eq. (4.17) to express β in terms of α; that is,

$$\beta = \frac{\alpha}{1-\alpha} \qquad (4.19)$$

Where, alpha is called common base current gain since it is very small. Typically alpha is always less than 1.

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_S \qquad (4.20)$$

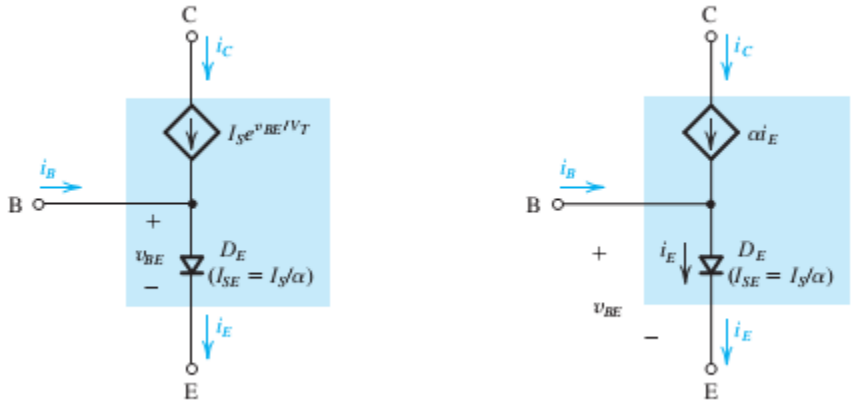


Fig. 4.4: Large signal equivalent circuit models of *npn* operating in forward active mode

4.1.3 Structure of actual transistors

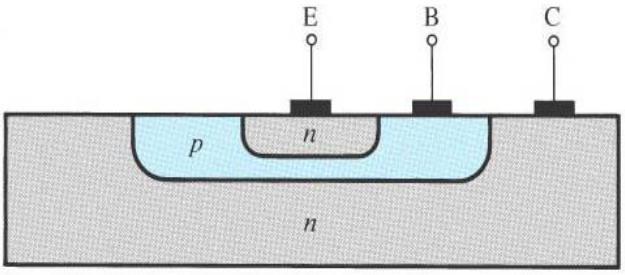


Fig. 4.5: Cross-section of an *npn* BJT

4.1.4 The Ebers-Moll (EM) model

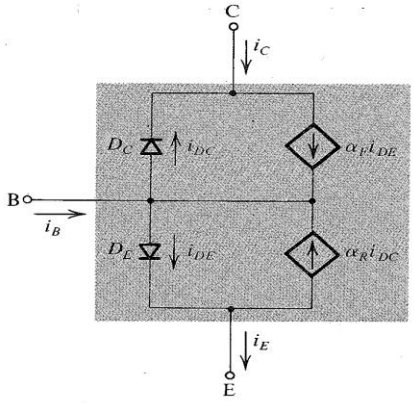


Fig. 4.6: Ebers-Moll model of *npn* transistor

- Eber proposed this compatible model to predict the operation of the BJT in all it's possible modes of operation. The collector and emitter currents can be given as

$$i_E = i_{DE} - \alpha_R i_{DC} \quad (4.21)$$

$$i_C = -i_{DC} + \alpha_F i_{DE} \quad (4.22)$$

$$i_B = (1-\alpha_F) i_{DE} + (1-\alpha_R) i_{DC} \quad (4.23)$$

Then we use the diode equation to express i_{DE} and i_{DC} as

$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1) \quad (4.24)$$

$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1) \quad (4.25)$$

Substituting for i_{DE} and i_{DC} in Eqs. (4.21), (4.22), and (4.23) and using the relationship in

Eq. (4.20) yield the required expressions:

$$i_E = \left(\frac{I_S}{\alpha_F}\right)(e^{v_{BE}/V_T} - 1) - I_S(e^{v_{BC}/V_T} - 1) \quad (4.26)$$

$$i_C = I_S(e^{v_{BE}/V_T} - 1) - \left(\frac{I_S}{\alpha_R}\right)(e^{v_{BC}/V_T} - 1) \quad (4.27)$$

$$i_B = \left(\frac{I_S}{\beta_F}\right)(e^{v_{BE}/V_T} - 1) + \left(\frac{I_S}{\beta_R}\right)(e^{v_{BC}/V_T} - 1) \quad (4.28)$$

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad (4.29)$$

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \quad (4.30)$$

As a first application of the EM model is to use it to predict the terminal currents of a transistor operating in the forward active mode. Here v_{BE} is positive and in the range of 0.6 V to 0.8 V, and v_{BC} is negative. One can easily see that terms containing $e^{vBC/VT}$ will be negligibly small and can be neglected to obtain

$$i_E \cong \left(\frac{I_S}{\alpha_F}\right)e^{v_{BE}/V_T} + I_S\left(1 - \frac{1}{\alpha_F}\right) \quad (4.31)$$

$$i_C \cong I_S e^{v_{BE}/V_T} + I_S\left(\frac{1}{\alpha_R} - 1\right) \quad (4.32)$$

$$i_B \cong \left(\frac{I_S}{\beta_F}\right)e^{v_{BE}/V_T} - I_S\left(\frac{1}{\beta_F} + \frac{1}{\beta_R}\right) \quad (4.33)$$

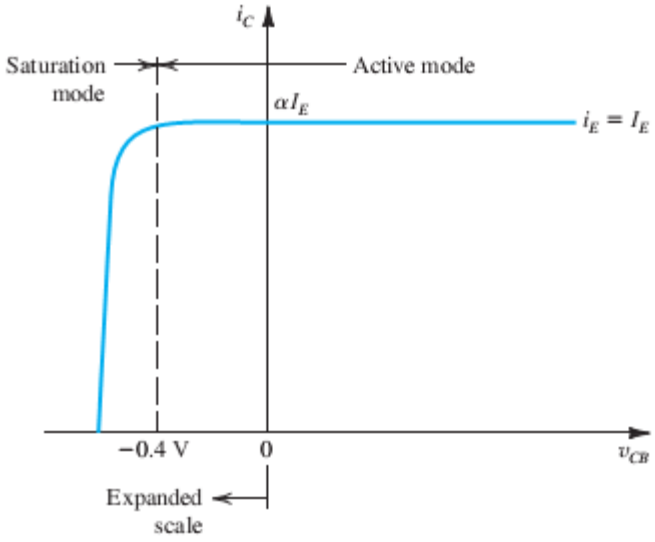


Fig.4.6: The i_C-v_{CB} characteristic of an npn transistor fed with a constant emitter current I_E. The transistor enters the saturation mode of operation for v_{CB} < -0.4 V, and the collector current diminishes.

4.1.5 Operation in the saturation mode

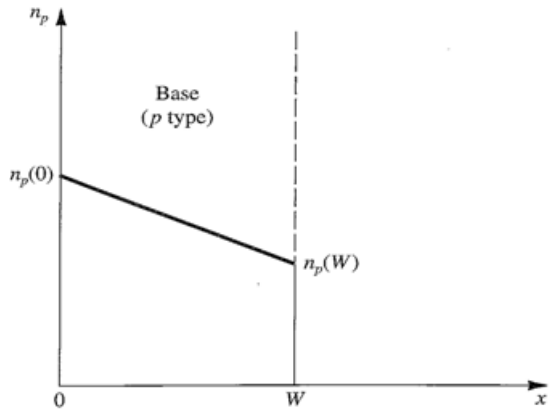


Fig. 4.7: Concentration profile of the minority carriers (electrons) in the base of an *npn* transistor operating in the saturation mode.

- When v_{CB} is lower than 0.4 V the transistor enters into saturation mode. Then current equation from Ebers Moll model can be given by

$$i_C = I_S e^{v_{BE}/V_T} - \left(\frac{I_S}{\alpha_R}\right) e^{v_{BC}/V_T} \qquad (4.34)$$

- The first term is a resultant current of Emitter base junction and the second term is the resultant of forward bias of collector base junction. The second term plays important role when υ_{BC} exceeds 0.4V.

4.1.6 The pnp transistor

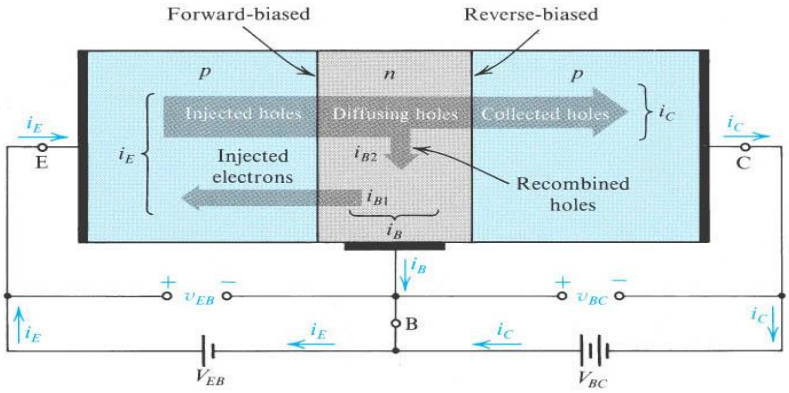


Fig. 4.8: Current flow in a *pnp* transistor biased to operate in the active mode.

- The pnp transistor usually works in active mode of operation. The voltage υ_{EB} causes p-type more potential than n-type which makes it forward bias (base-emitter junction). The collector-base junction is reverse biased by the voltage $\upsilon_{BC.}$
- Unlike in pnp transistor the current is mainly due to holes in pnp transistor.

4.2 Current–Voltage Characteristics

4.2.1 Circuit symbols and conventions

- The polarity of the device (pnp or npn) is indicated by the direction of the arrowhead on the emitter.
- The current flows from top to bottom and voltages are high at top and lower at bottom.
- An npn transistor whose EBJ is forward biased will operate in the active mode as long as the collector voltage does not fall below that of the base by more than approximately 0.4V.
- The current denoted I_{CBO} is the reverse current flowing from collector to base with the emitter open-circuited.

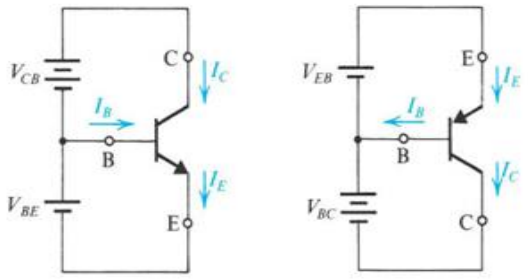


Fig. 4.9: Voltage polarities and current flow in transistors biased in the active mode

4.2.2 Graphical representation of Transistor characteristics

- The exponential relationship between the i_c and υ_{BE} is as follows

$$i_C = I_S e^{\upsilon_{BE}/V_T}$$

- The i_c- V_{BE} characteristics of a npn transistor are as follows:

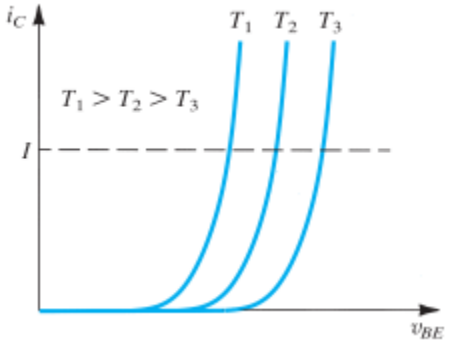


Fig. 4.10: Effect of temperature on the i_C–υ_{BE} characteristic. At a constant emitter current (broken line), υ_{BE} changes by –2 mV/°C.

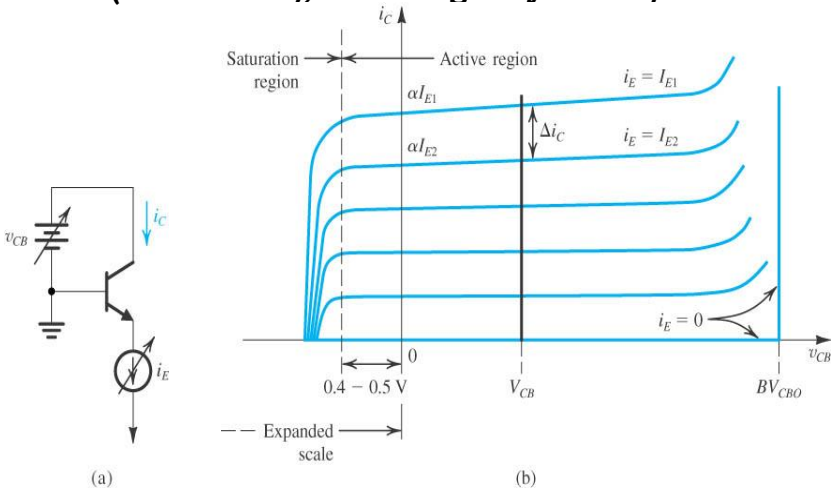


Fig. 4.11: The i_C–v_{CB} characteristics of an *npn* transistor

- For a pnp transistor, the characteristics will be identical with v_{BE} replaced with v_{EB}.
- The common base characteristics are the plots between i_C and v_{CB} for various values of i_E is as follows
- Each of the characteristic curves intersect the vertical axis at the current level equal to αI_E

$$i_C = \alpha_F I_E - I_S\left(\frac{1}{\alpha_R} - \alpha_F\right)e^{v_{BC}/V_T} \qquad (4.35)$$

4.2.3 Dependence of i_C on the collector voltage: The Early effect

- At low values of v_{CE} as the collector voltage goes below that of the base by more than 0.4V the collector base junction becomes forward biased and transistor leaves active mode and enters saturation mode.
- The characteristic lines meet at a point on the negative v_{CE} axis, at v_{CE}=-V_A. The voltage V_A is called Early voltage.
- At a given value of v_{BE}, increasing v_{EC} increases the reverse-bias voltage on the collector-base junction and thus increases the width of the depletion region.
- This in turn results in a decrease in the effective base width W. This is the Early effect.

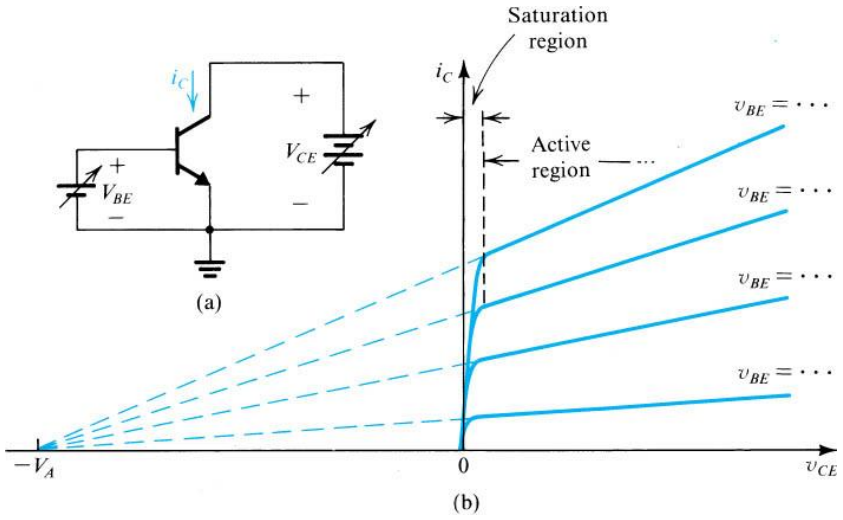


Fig. 4.12: (a) Conceptual circuit for measuring the i_C–v_{CE} characteristics of the BJT. (b) The i_C–v_{CE} characteristics of a practical BJT.

- The linear dependence of i_c on v_{CE} can be accounted for by assuming that I_s remains constant and including the factor $(1+V_{ce}/V_A)$ in the equation for i_C as follows

$$i_C = I_S e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right) \qquad (4.36)$$

The nonzero slope of the ic-V_{CE} straight lines indicates that the output resistance looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o \equiv \left[\left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=\text{constant}}\right]^{-1} \qquad (4.37)$$

Using Eq. (4.36) we can show that

$$r_o = \frac{V_A + V_{CE}}{I_C} \qquad (4.38)$$

where Ic and V_{CE} are the coordinates of the point at which the BJT is operating on the particular ic-v_{CE} curve (i.e., the curve obtained for $v_{BE} = V_{BE}$). Alternatively, we can write

$$r_o = \frac{V_A}{I'_C} \qquad (4.38a)$$

where I'_C is the value of the collector current with the Early effect neglected; that is,

$$I'_C = I_S e^{V_{BE}/V_T} \qquad (4.38b)$$

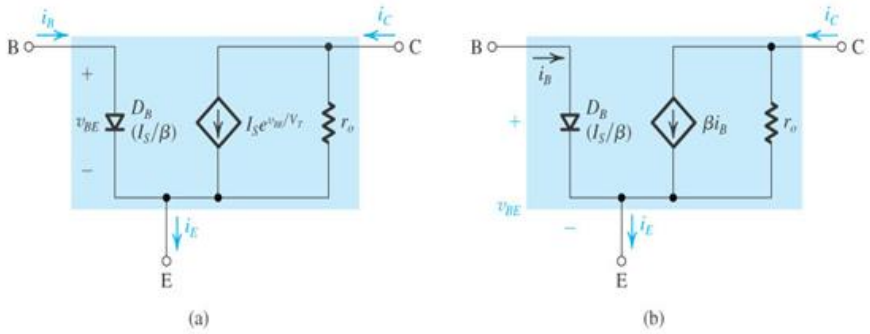


Fig. 4.13: Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration.

4.2.4 Common-Emitter Characteristics

- The base current i_B rather than base-emitter voltage v_{BE} is used as parameter here.
- β is the common emitter current gain, it is the ratio of total current in collector to the total current in the base.
- The common emitter characteristics are shown below in Figure 4.14.

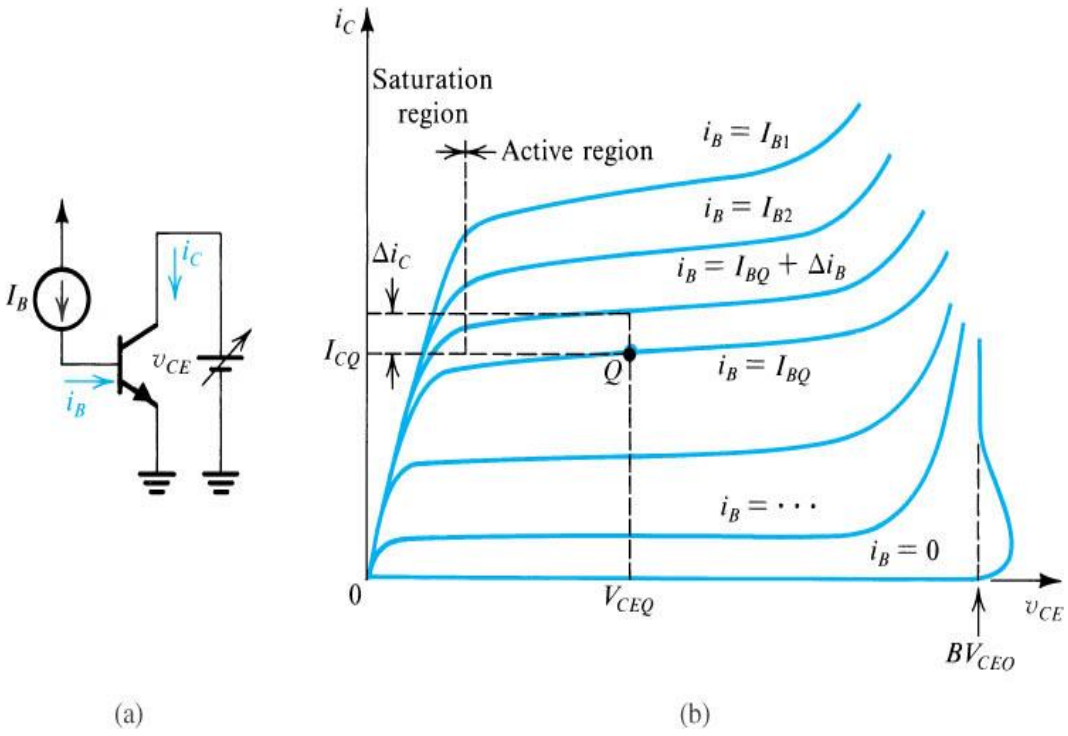


Fig. 4.14: Common-emitter characteristics. Note that the horizontal scale is expanded around the origin to show the saturation region in some detail.

- Consider a transistor operating in the active region at the point labeled Q in Fig. 4.21, that is, at a collector current I_{CQ}, a base current I_{BQ}, and a collector-emitter voltage V_{CEQ}. The ratio of the collector current to the base current is the large-signal or dc β,

$$\beta_{dc} \equiv \frac{I_{CQ}}{I_{BQ}} \qquad (4.39)$$

- While keeping v_{CE} constant at the value V_{CEQ}, changing i_B from I_{BQ} to iJBQ + AiB)

  results in i_C increasing from I_{CQ} to (I_{CQ} + Aic). Thus we can define the incremental or ac β,

$$\beta_{ac} = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{v_{CE}=\text{constant}} \qquad (4.40)$$

- The magnitudes of β_{ac} and β_{dc} differ, typically by approximately 10% to 20%.

The Saturation Voltage V_{CE}sat and Saturation Resistance R_{CE}sat

An expanded view of the common-emitter characteristics in the saturation region is shown in Fig. 4.15. The fact that the curves are "bunched" together in the saturation region implies that the incremental β is lower there than in the active region.

- A possible operating point in the saturation region is that labeled X. It is characterized by a base current I_B, *a* collector current I_C sat , and a collector-emitter voltage $V_{CE}sat$.
- A saturated transistor is said to be operating at a forced β given by

$$\beta_{\text{forced}} \equiv \frac{I_{C\,\text{sat}}}{I_B} \qquad (4.41)$$

$$\beta_{\text{forced}} < \beta_F \qquad (4.42)$$

- The ratio of [β_F to β forced] is known as the overdrive factor.
- The greater the overdrive factor, the deeper the transistor is driven into saturation and the lower V_{CE} sat becomes.

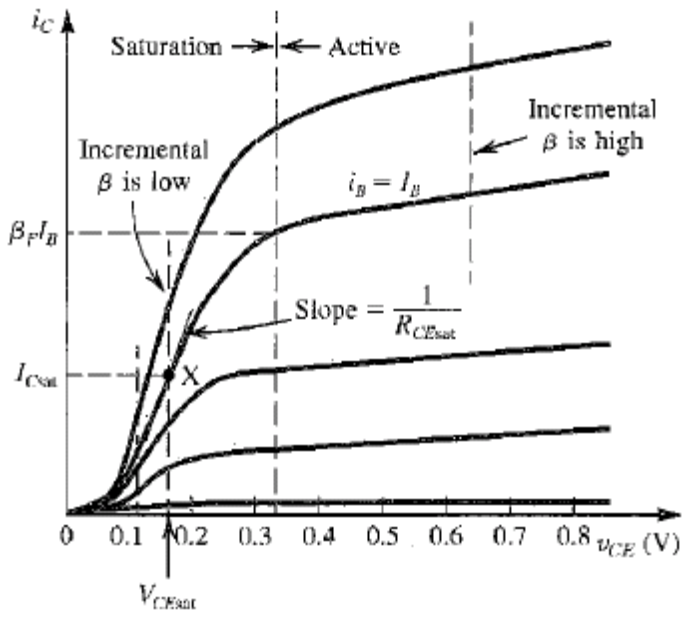


Fig.4.15: An expanded view of the common-emitter characteristics in the saturation region.

- The i_C-v_{CE} curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance R_{CE}sat,

$$R_{CEsat} \equiv \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{\substack{i_B=I_B \\ i_C=I_{Csat}}} \qquad (4.43)$$

- The ic-v_{CE} characteristic curves of the saturated transistor shown in Fig. 4.16(a). It is interesting to note that the curve intersects the v_{CE} axis at V_T ln $(1/\alpha_R)$, a value common to all the i_C-v_{CE} curves.
- We have also shown in Fig. 4.16 (b), the tangent at operating point X of slope $1/R_{CE}$ sat. When extrapolated, the tangent intersects the V_{CE}-axis at a voltage V_{CE}off, typically approximately 0.1 V.

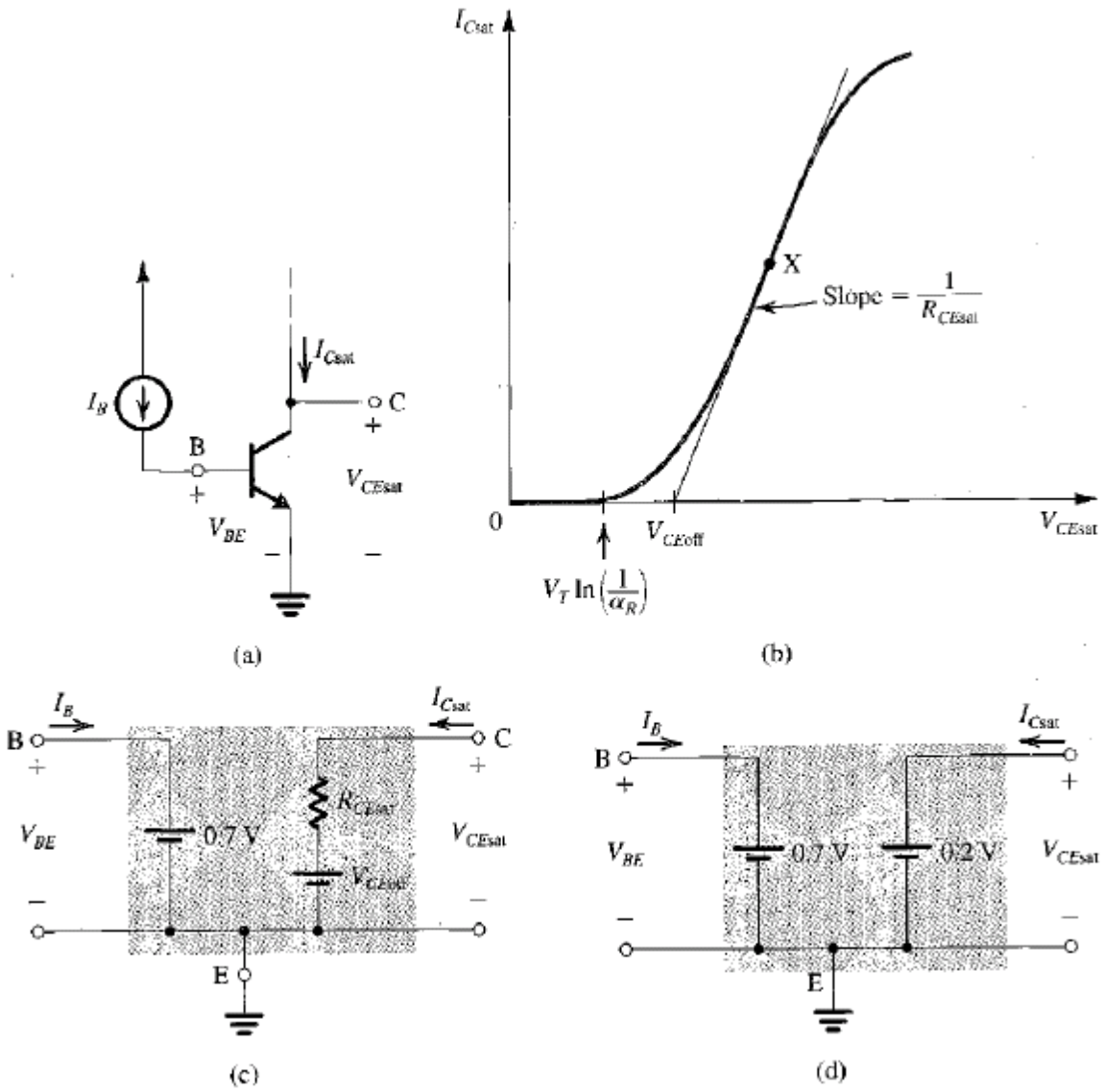


Fig.4.16: (a) An npn transistor operated in saturation mode with a constant base current I_B. (b) The ic-v_{CE} characteristic curve corresponding to $i_B = I_B$. The curve can be approximated by a straight line of slope $1/R_{CE}$ sat (c) Equivalent-Circuit representation of the saturated transistor, (d) A simplified equivalent circuit model of the saturated transistor.

- It follows that the ic-v_{CE} characteristic of a saturated transistor can be approximately represented by the equivalent circuit shown in Fig. 4.16(c). At the

collector side, the transistor is represented by a resistance R_{CE}sat in series with a battery V_{CE}off. Typically, V_{CE} sat falls in the range of 0.1 V to 0.3 V. Thus the saturation voltage V_{CE} sat can be found from

$$V_{CEsat} = V_{CEoff} + I_{Csat} R_{CEsat} \qquad (4.44)$$

- The value of β depends on I_C an on temperature and it is plotted as follows:

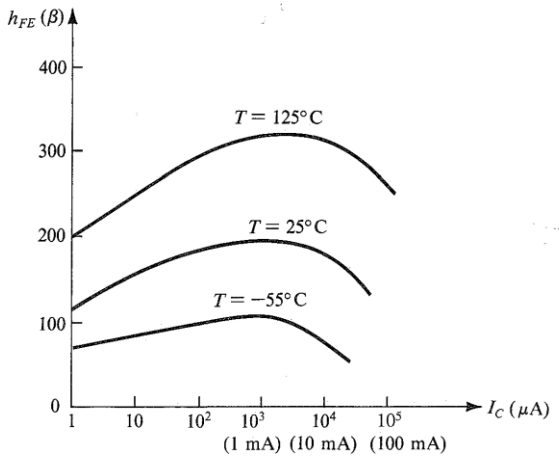


Fig. 4.17: Typical dependence of β on I_C and on temperature in a modern integrated-circuit *npn* silicon transistor intended for operation around 1 mA.

4.2.5 Transistor Breakdown

- The i_C-v_{CB} characteristics indicate that for I_E =0 , the collector-base junction breaks down at a voltage denoted by BVCBO
- These effects on characteristics are more complex in common-base configuration. V_{CEO} is referred as sustaining voltage.
- The breakdown of CBJ in either modes is not destructive as long as the power dissipation in the device is kept within safe limits.
- The EBJ breaks down in an avalanche manner at a voltage BV_{BEO} smaller than BV_{CBO}.

4.3 The BJT as an amplifier and as a switch

- The two major applications of BJT are signal amplifier, and as a digital-circuit switch. The basis for the amplifier application is the fact that when the BJT is operated in the active mode, it acts as a voltage-controlled current source.

a) Changes in the base-emitter voltage v_{BE} gives rise to changes in the collector current ic. Thus in the active mode the BJT can be used to implement a trans-conductance amplifier. Voltage amplification can be obtained simply by passing the collector current through a resistance Rc.

b) Since the collector current ic is exponentially related to v_{BE}, we will bias the transistor to operate at a dc base-emitter voltage V_{BE} and a corresponding dc collector current I_C.

c) Then superimpose the signal to be amplified, vbe, on the dc voltage V_{BE}. By keeping the amplitude of the signal v_{be} small, we will be able to constrain the transistor to operate on a short, almost linear segment of the ic-v_{BE} characteristic. Thus, the change in collector current, ic, will be linearly related to vbe.

d) From the transfer characteristic of the circuit, we will be able to see clearly the region over which the circuit can be operated as a linear amplifier. We also will be able to see how the BJT can be employed as a switch.

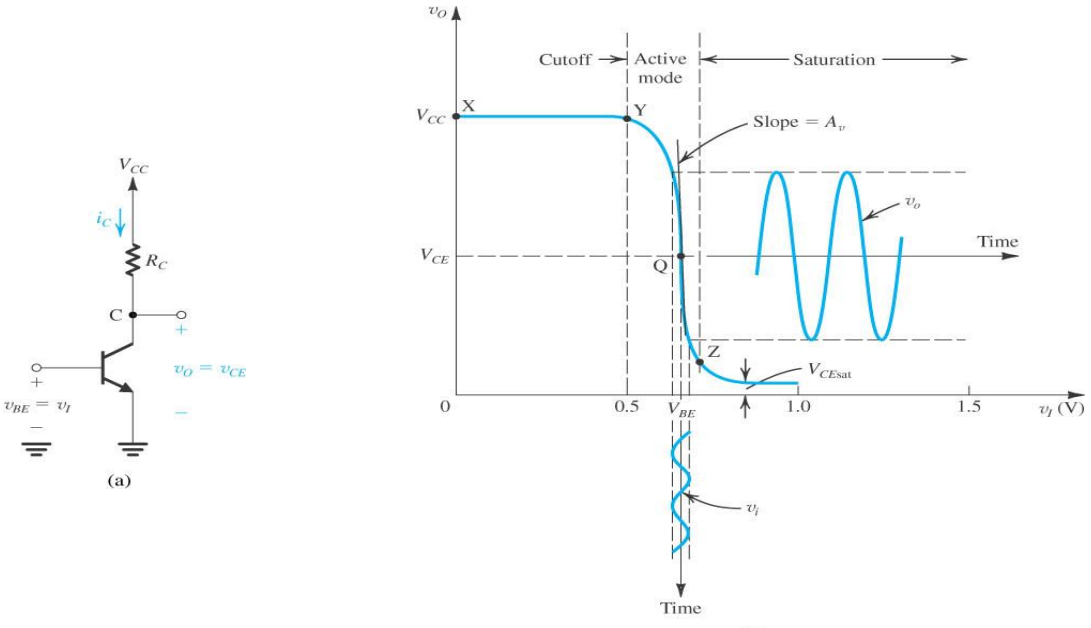


Fig. 4.18: (a) Basic common-emitter amplifier circuit (b) Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal v_I is superimposed on the dc bias voltage V_{BE}. The resulting output signal $v_O$appears superimposed on the dc collector voltage V_{CE}. The amplitude of $v_O$is larger than that of v_I by the voltage gain A_v.

4.3.1 Amplifier Gain

- To operate the BJT as a linear amplifier, it must be biased at a point in the active region. Figure 4.18 (b) shows such a bias point, labeled Q (for quiescent point), and characterized by a dc base-emitter voltage V_{BE} and a dc collector-emitter voltage V_{CE}. If the collector current at this value of V_{BE} is denoted I_C , that is,

$$I_C = I_S e^{V_{BE}/V_T} \tag{4.45}$$

then from the circuit in Fig. 4.18(a) we can write

$$V_{CE} = V_{CC} - R_C I_C \tag{4.46}$$

- If the signal to be amplified, v_I is superimposed on V_{BE} and kept sufficiently small, as indicated in Fig. 4.18(b), the instantaneous operating point will be constrained to a relatively short, almost-linear segment of the transfer curve around the bias point Q. The slope of this linear segment will be equal to the slope of the tangent to the transfer curve at Q. This slope is the voltage gain of the amplifier for small-input signals around Q.
- An expression for the small-signal gain A_V can be found by differentiating the expression in Eq. (5.2) and evaluating the derivative at point Q; that is, for $v_I = V_{BE}$,

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{BE}} \tag{4.47}$$

$$v_O = V_{CC} - R_C I_S e^{v_I/V_T}$$

$$A_v = -\frac{1}{V_T} I_S e^{V_{BE}/V_T} R_C$$

using Eq. (4.45), we can express A_V in compact form:

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T} \tag{4.48}$$

Where, V_{RC} is the dc voltage drop across R_C,

$$V_{RC} = V_{CC} - V_{CE} \tag{4.49}$$

- Observe that the CE amplifier is inverting; that is, the output signal is 180° out of phase relative to the input signal. The simple expression in Eq. (4.48) indicates that the voltage gain of the common-emitter amplifier is the ratio of the dc voltage drop across R_C to the thermal voltage V_T (= 25 mV at room temperature). It follows

that to maximize the voltage gain we should use as large a voltage drop across R_C as possible.

- For a given value of V_{CC}, Eq. (4.49) indicates that to increase V_{RC} we have to operate at a lower V_{CE}. However, reference to Fig. 4.18 (b) shows that a lower V_{CE} means a bias point Q close to the end of the active region segment, which might not leave sufficient room for the negative-output signal swing without the amplifier entering the saturation region. If this happens, the negative peaks of the waveform of v_0 will be flattened.
- It is the need to allow sufficient room for output signal swing that determines the most effective placement of the bias point Q on the active-region segment, YZ, of the transfer curve.
- Placing Q too high on this segment not only results in reduced gain (because V_{RC} is lower) but could possibly limit the available range of positive signal swing. At the positive end, the limitation is imposed by the BJT cutting off, in which event the positive-output peaks would be clipped off at a level equal to VCC.
- Finally, it is useful to note that the theoretical maximum gain A_V is obtained by biasing the BJT at the edge of saturation, which of course would not leave any room for negative signal swing. The resulting gain is given by

$$A_v = -\frac{V_{CC} - V_{CE\text{sat}}}{V_T} \qquad (4.50)$$

$$A_{v\max} \cong -\frac{V_{CC}}{V_T} \qquad (4.51)$$

- Although the gain can be increased by using a larger supply voltage, other considerations come into play when determining an appropriate value for V_{CC}. In fact, the trend has been toward using lower and lower supply voltages, currently approaching 1 V or so. At such low supply voltages, large gain values can be obtained by replacing the resistance R_C with a constant-current source.

4.3.2 Operation as a Switch

- To operate the BJT as a switch, we utilize the cutoff and the saturation modes of operation. To illustrate, consider once more the common-emitter circuit shown in Fig. 4.19 as the input v_I is varied.

- For v_I less than about 0.5 V, the transistor will be cut off; thus $i_B = 0$, $i_C = 0$, and $v_C = V_{CC}$. In this state, node C is disconnected from ground; the switch is in the open (OFF) position.
- To turn the transistor ON, we have to increase $\boldsymbol{v_I}$ above 0.5 V. In fact, for appreciable

  currents to flow, v_{BE} should be about 0.7 V and $\boldsymbol{v_I}$ should be higher. The base current will be

$$i_B = \frac{v_I - V_{BE}}{R_B} \qquad (4.52)$$

  and the collector current will be $i_C = \beta\, i_B$ (4.53)

  which applies only when the device is in the active mode. This will be the case as long as the CBJ is not forward biased, that is, as long as $v_C > v_B$ - 0.4 V, where $\boldsymbol{v_C}$ is given by

$$v_C = V_{CC} - i_C R_C \qquad (4.54)$$

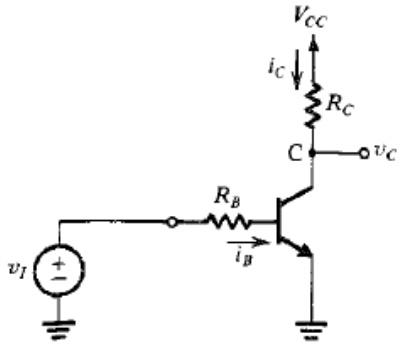


Fig. 4.19: A simple circuit used to illustrate the different modes of operation of the BJT.

- As $\boldsymbol{v_I}$ is increased, i_B will increase (Eq. 4.52), i_C will correspondingly increase (Eq. 4.53), and v_C will decrease (Eq.4.54). Eventually, v_C will become lower than v_B by 0.4 V, at which point the transistor leaves the active region and enters the saturation region. This edge-of-saturation (EOS) point is defined by

$$I_{C(EOS)} = \frac{V_{CC} - 0.3}{R_C} \qquad (4.55)$$

  Where, assume that V_{BE} is approximately 0.7 V, and

$$I_{B(\text{EOS})} = \frac{I_{C(\text{EOS})}}{\beta} \qquad (4.56)$$

The corresponding value of v_I required to drive the transistor to the edge-of-saturation canbe found from

$$V_{I(\text{EOS})} = I_{B(\text{EOS})}R_B + V_{BE} \qquad (4.57)$$

- Increasing v_I above $v_I(EOS)$ increases the base current, which drives the transistor deeper into saturation. The collector-to-emitter voltage, however, decreases only slightly. As a reasonable approximation, we shall assume that for a saturated transistor, V_{CE} *(sat)* is approximately equal to 0.2 V. The collector current then remains nearly constant at I_C *(sat),*

$$I_{C\text{sat}} = \frac{V_{CC} - V_{CE\text{sat}}}{R_C} \qquad (4.58)$$

- Forcing more current into the base has very little effect on I_C *(sat)* and V_{CE} *(sat).* In this state the switch is closed (ON), with a low closure resistance R_{CE} *(sat)* and a small offset voltage V_{CE} *off.*
- Finally, in saturation one can force the transistor to operate at any desired β below the normal value; that is, the ratio of the collector current I_C *(sat)* to the base current can be set at will and is therefore called the forced β,

$$\beta_{\text{forced}} \equiv \frac{I_{C\text{sat}}}{I_B} \qquad (4.59)$$

The ratio of I_B to I_B *(EOS)* is known as the overdrive factor.

UNIT – 5

Biasing of MOSFET and BJT

Syllabus: Biasing of BJTs - operating point, fixed-bias circuit, emitter-stabilized bias circuit, voltage-divider bias, dc bias with voltage feedback, bias stabilization, design of voltage-divider bias circuit from bias stability considerations, Biasing of E-MOSFETs : Drain-feedback configuration, E-MOSFET voltage - divider configuration.

5.1 INTRODUCTION

- Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies.
- The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion.
- Although a number of networks are analyzed but there is a similarity between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$V_{BE} = 0.7\ V$$
$$I_E = (1+\beta)I_B + I_C$$
$$I_C = \beta I_B$$

Need for Biasing

- The process of giving proper supply voltages and resistances for obtaining the desired Q-Point is called Biasing. The circuits used for getting the desired and proper operating point are known as biasing circuits.
- To establish the operating point in the active region biasing is required for transistors to be used as an amplifier.
- For analog circuit operation, the Q-point is placed so the transistor stays in active mode (does not shift to operation in the saturation region or cut-off region) when input is applied.
- For digital operation, the Q-point is placed so the transistor does the contrary - switches from "on" to "off" state.
- Q-point is established near the center of active region of transistor characteristic to allow similar signal swings in positive and negative directions.

- Q-point should be stable. In particular, it should be insensitive to variations in transistor parameters (for example, should not shift if transistor is replaced by another of the same type), variations in temperature, variations in power supply voltage.

5.2 OPERATING POINT

- In order to produce distortion free output in amplifier circuits, the supply voltages and resistances establish a set of dc voltage V_{CEQ} and I_{CQ} to operate the transistor in the active region.
- These voltages and currents are called quiescent values which determine the operating point or Q-point for the transistor.
- DC biasing is used to establish proper values of I_C and V_{CE} called the DC operating point or quiescent point or *Q*-point.

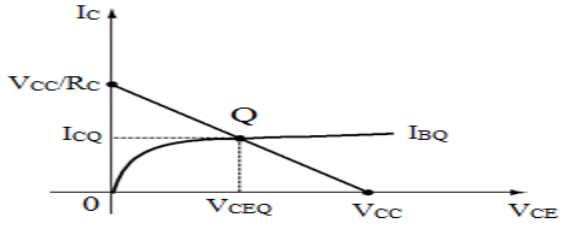


Fig.5.1: Load line analysis

- Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point) (quiescent means quiet, still, inactive)
- Figure 5.2 shows a general output device characteristic with four operating points indicated.

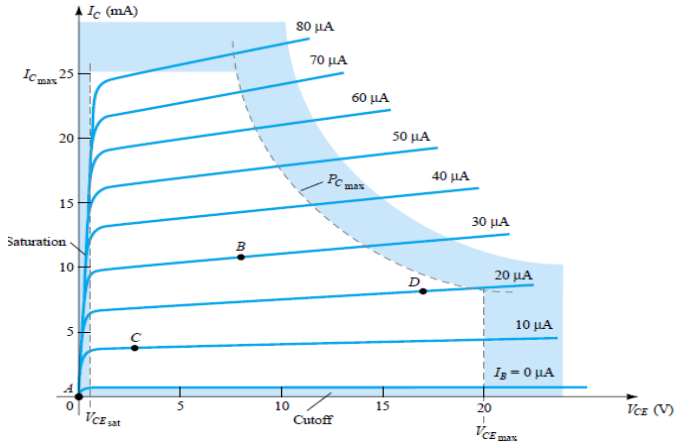


Fig.5.2:

- The maximum ratings are indicated on the characteristics of Fig. 5.2 by a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax}. The maximum power constraint is defined by the curve P_{Cmax} in the same figure.
- The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device.
- If no bias were used, the device would initially be completely off, resulting in a **Q-point at A**—namely, zero current through the device (and zero voltage across it).
- For **point B**, if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal.
- **Point C** would allow some positive and negative variation of the output signal, but the peak to-peak value would be limited by the proximity of V_{CE} =0v/I_C = 0 mA.
- **Point D** sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded.
- **Key point**: Point B (as shown in Fig. 5.2) therefore seems the best operating point in terms of linear gain (constant) and largest possible voltage and current swing.
- Having selected and biased the BJT at a desired operating point, Temperature causes the device parameters such as the transistor current gain (βac) and the transistor leakage current (I_{CEO}) may change, thereby changing the operating condition set by the biasing network.
- Therefore the biasing network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point.
- This maintenance of the operating point can be specified by a **stability factor, S**, which indicates the degree of change in operating point due to a temperature variation.
- Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:
    1. Linear-region operation:
        a) . The base–emitter junction must be forward-biased (p-region voltage more positive),with a resulting forward-bias voltage of about 0.6 to 0.7 V.
        b) The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.
    2. Cutoff-region operation: Base–emitter junction reverse biased
    3. Saturation-region operation:
       Base–emitter junction forward biased and Base–collector junction forward biased.

5.3 FIXED-BIAS CIRCUIT

- The fixed-bias technique relatively straight forward and simple for dc bias analysis. Fixed bias circuit is shown in Fig: 5.3

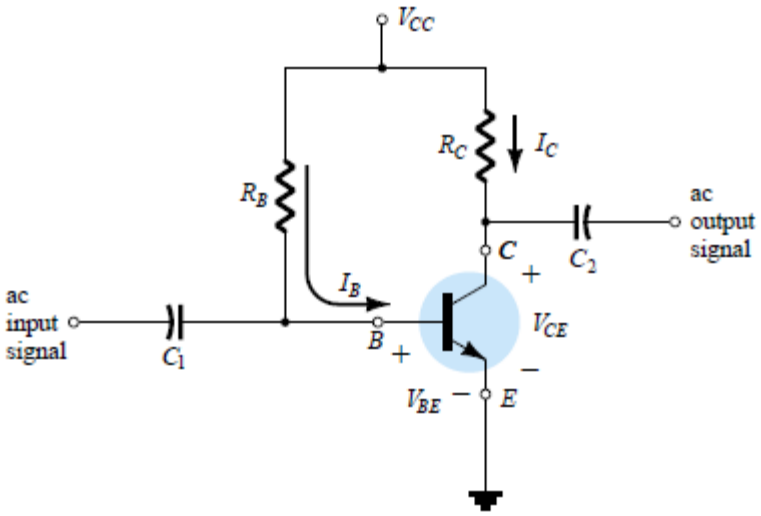


Fig.5.3: Fixed bias circuit

- For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open circuit equivalent and the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 5.4 to permit a separation of input and output circuits.

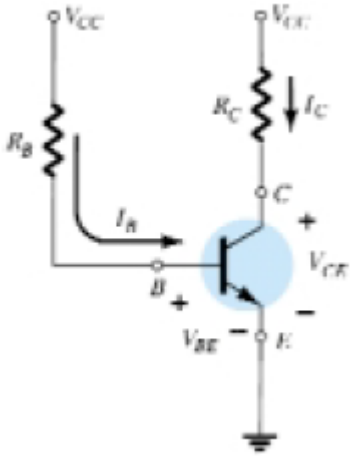


Fig.5.4: D.C equivalent of Fixed bias circuit

- **Forward Bias of Base–Emitter :** Consider first the base–emitter circuit loop of Fig. 5.5. Writing Kirchhoff's voltage equation in the clockwise direction for the loop.
- we obtain

$$V_{CC} - I_B R_B - V_{BE} = 0$$

- Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}).
- Since the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor, R_B, sets the level of base current for the operating point.

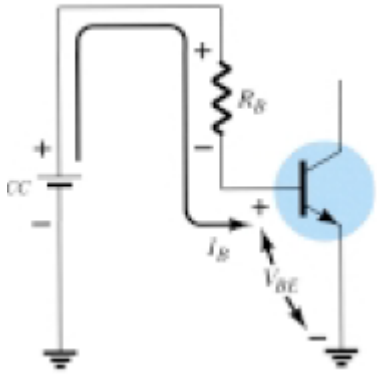


Fig.5.5:**Base emitter loop**

- **Collector–Emitter Loop:** The collector–emitter section of the network appears in Fig. 5.6 with the indicated direction of current I_C and the resulting polarity across R_C.
- The magnitude of the collector current is related directly to I_B through

$$Ic=\beta I_B$$

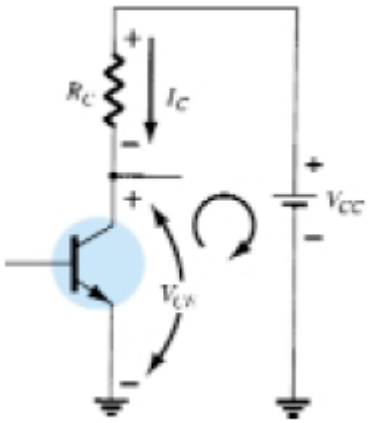


Fig.5.6: **Collector emitter loop**

- **Note:** Since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.
- Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 5.6 will result in , $V_{CE} - I_C R_C - V_{CC} = 0$

$$V_{CE} = V_{CC} - I_C R_C$$

- But in this case, since $V_E = 0$ V, we have

$$V_{CE} = V_C$$

- In addition, since $V_{BE} = V_B - V_E$ and $V_E = 0$ V, then

$$V_{BE} = V_B$$

- **Transistor Saturation :**Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted.

- An operating point in the saturation region is depicted in Fig. 5.7.

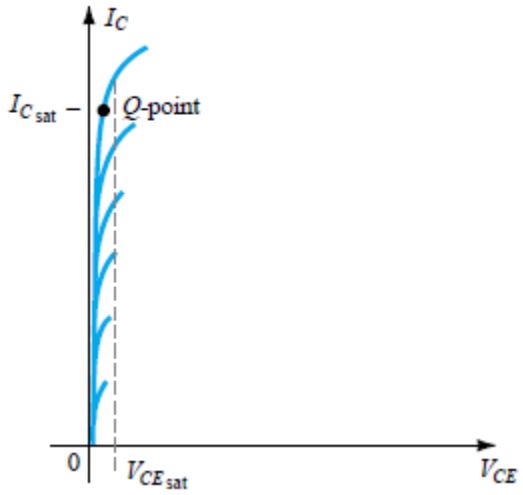


Fig.5.7:**Saturation region**

- Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE\text{sat}}$. In addition, the collector current is relatively high on the characteristics and the voltage V_{CE} is assumed to be zero volts.
- If there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor shown in fig 5.8 and calculate the resulting collector current. In short, set V_{CE} = 0 V.

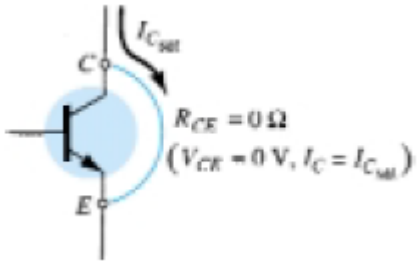


Fig.5.8:Determine Ic_{sat}

- The resulting saturation current for the fixed-bias configuration is

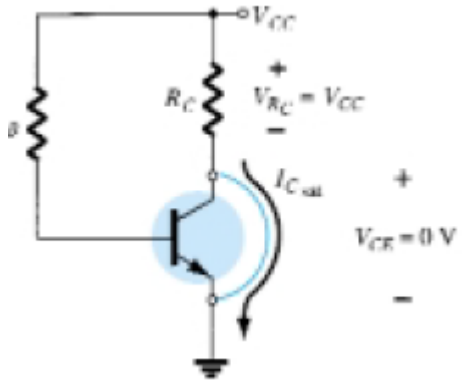


Fig.5.9: Determining Icsat for fixed bias circuit

- Once I_{Csat} is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.
- **Load-Line Analysis :**We will now investigate how the network parameters define the possible range of *Q*-points and how the actual *Q*-point is determined.
- The network of Fig. 5.10 establishes an output equation that relates the variables *IC* and *VCE* in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

- The output characteristics of the transistor also relate the same two variables I_C and V_{CE} shown in Fig. 5.10

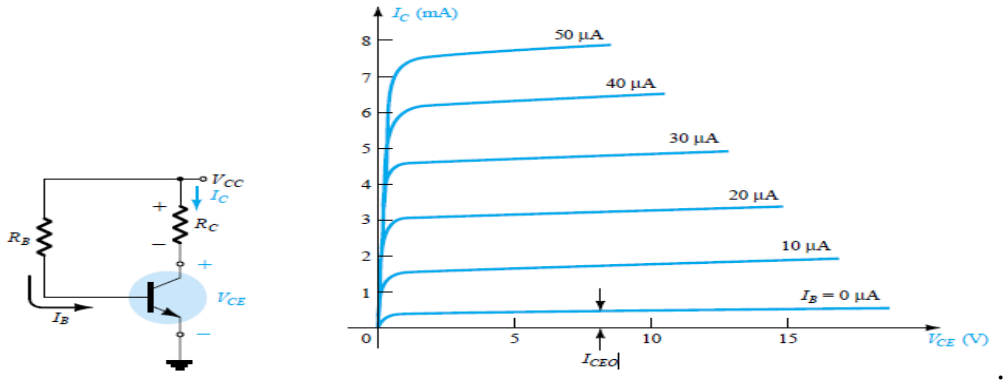


Fig.5.10: Fixed bias circuit and output characteristics

- If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} \_ I_C R_C$$

And

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{ce} = 0\,V} \quad \ldots\ldots\ldots\ldots(5.1)$$

- If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. We can find that

$$V_{CE} = V_{CC} \_ (0) R_C$$

and

$$V_{CE} = V_{CC} \ldots\ldots\ldots\ldots\ldots\ldots (5.2)$$

- By joining the two points defined by Eqs. (5.1) and (5.2), the straight line established. The resulting line on the graph of Fig. 5.10 is called the *load line* since it is defined by the load resistor R_C.
- By solving for the resulting level of I_B, the actual *Q*-point can be established as shown in Fig. 5.11

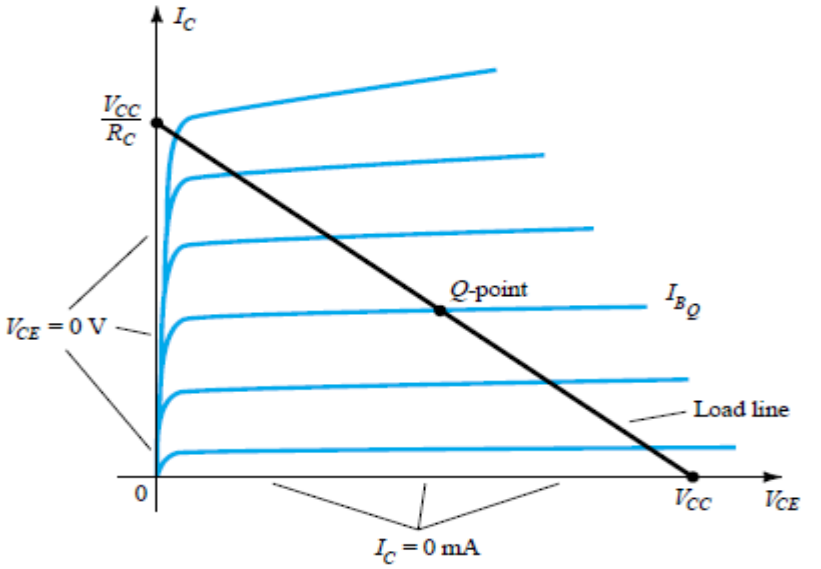


Fig.5.11: Fixed bias load line

- If the level of I_B is changed by varying the value of R_B the Q-point moves up or down the load line as shown in Fig. 5.12.

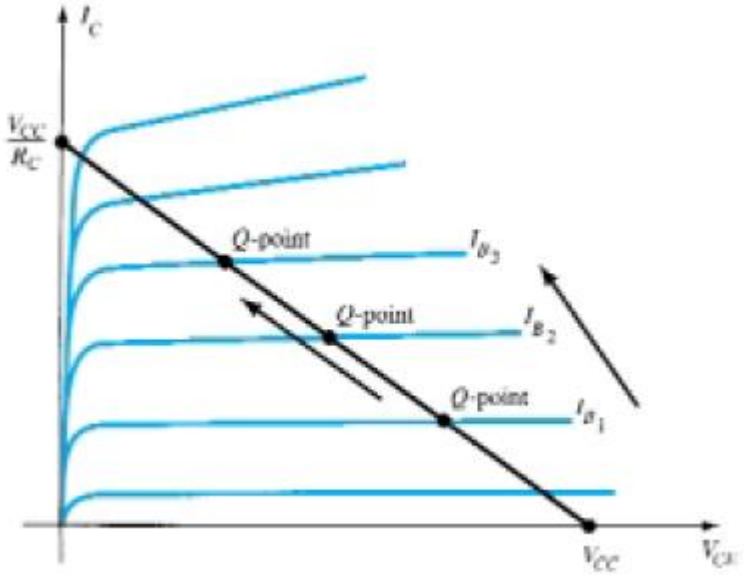


Fig.5.12: Movement of *Q*-point with increasing levels of I_B

- If V_{CC} is held fixed and R_C changed, the load line will shift as shown in Fig. 5.13. If I_B is held fixed, the Q-point will move as shown in the same figure.

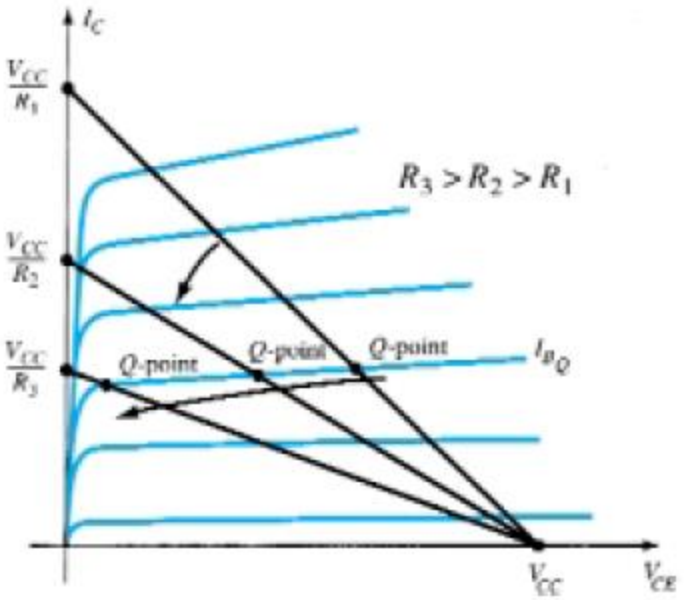


Fig.5.13: Effect of increasing levels of R_C on the load line and *Q*-point

- If R_C is fixed and V_{CC} varied, the load line shifts as shown in Fig. 5.14.

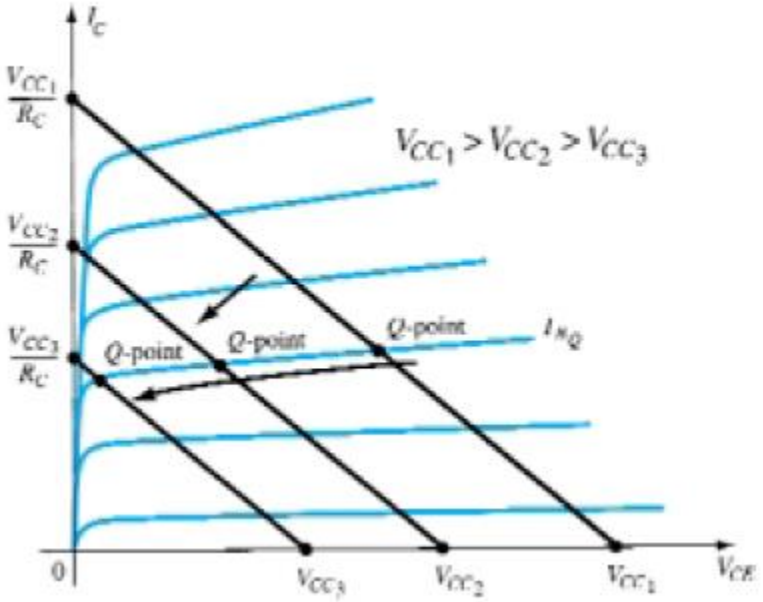


Fig.5.14: Effect of lower values of V_{CC} on the load line and *Q*-point

5.4 EMITTER-STABILIZED BIAS CIRCUIT

- The dc bias network of Fig. 5.15 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.

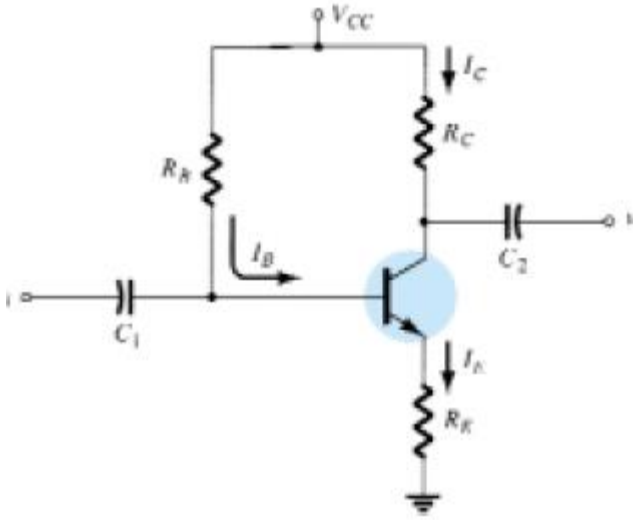


Fig.5.15: BJT bias circuit with emitter resistor.

- The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.
- **Base–Emitter Loop:** The base–emitter loop of the network of Fig. 5.15 can be redrawn as shown in Fig. 5.16.

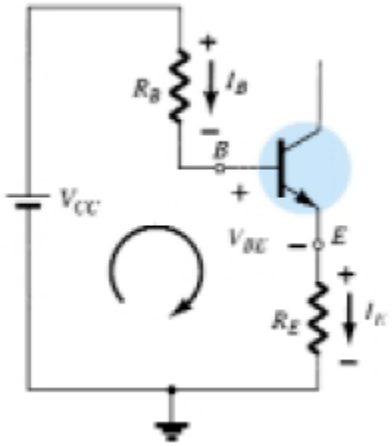


Fig.5.16: Base–emitter loop

- Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$VCC \_ I_BR_B \_ V_{BE} \_ I_ER_E = 0$ ……..(5.3)

$I_E = (1+\beta)I_B$

Substituting for I_E in Eq. (4.3) will result in

$V_{CC} \_ I_BR_B \_ V_{BE} \_ (1+\beta)I_BR_E = 0$

Grouping terms will then provide the following:

$-I_B(R_B + (1+\beta)R_E) + V_{CC} \_ V_{BE} = 0$

Multiplying through by (1+β) we have

$I_B(R_B + (1+\beta)R_E) \_ V_{CC} + V_{BE} = 0$

with

$I_B(R_B + (1+\beta)R_E) = V_{CC} \_ V_{BE}$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

- Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(1+\beta)R_E$.
- Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(1+\beta)$.

$$R_i=(1+\beta)R_E$$

- **Collector–Emitter Loop :** The collector–emitter loop is redrawn in Fig. 5.17

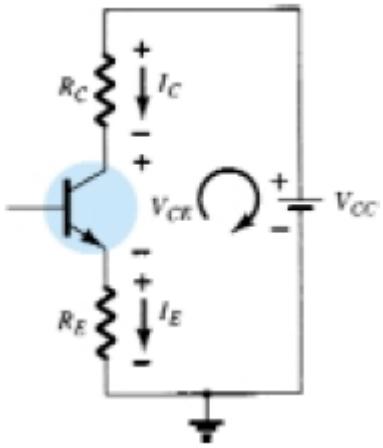


Fig.5.17: Collector–emitter loop

- Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in

$$I_E R_E + V_{CE} + I_C R_C \_ V_{CC} = 0$$

- Substituting $I_E = I_C$ and grouping terms gives

$$V_{CE} - V_{CC} - I_C(R_C + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

- The single-subscript voltage V_E is the voltage from emitter to ground and determined by $V_E = I_E R_E$
- while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E \text{ and } V_C = V_{CE} + V_E \text{ or } VC = V_{CC} + I_C R_C$$

- The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B \text{ or } V_B = V_{BE} - V_E)$$

- The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

- **Saturation Level :** The collector saturation level or maximum collector current for an emitter-bias design can be determined: By apply a short circuit between the collector–emitter terminals as shown in Fig.5.18 and calculate the resulting collector current.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

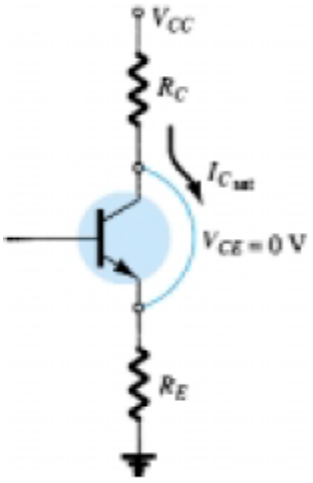


Fig.5.18: Determining I_{Csat} for the emitter-stabilized bias circuit.

- **Load-Line Analysis:** The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

- Choosing I_C=0 mA gives

$$V_{CE} = V_{CC} \text{ at } I_C = 0 \text{ mA}$$

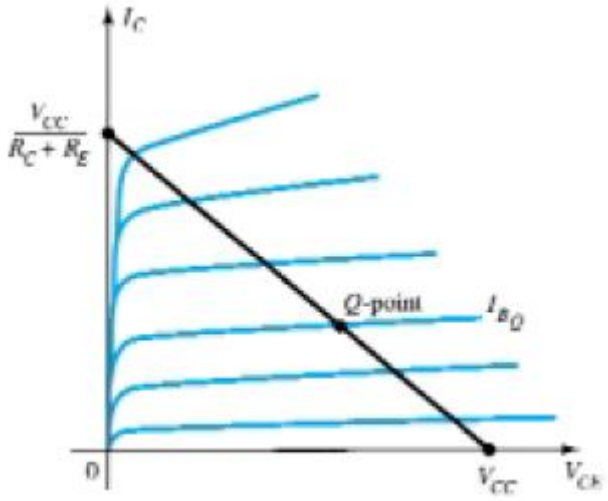


Fig.5.19: Load line for the emitter-bias configuration

- Different levels of I_{BQ} will, of course, move the Q-point up or down the load line can observe in Fig 5.19.

5.5 SELF-BIAS OR VOLTAGE DIVIDER BIAS

- The voltage divider is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction.
- By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β.
- In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current.
- Required base bias is obtained from the power supply through potential divider R_1& R_2.
- In this circuit voltage across reverse biases base emitter junction increases, voltage across R_E increases causing base current to diverse which compensate the increase in collector current. This circuit can be used with low collector resistance.

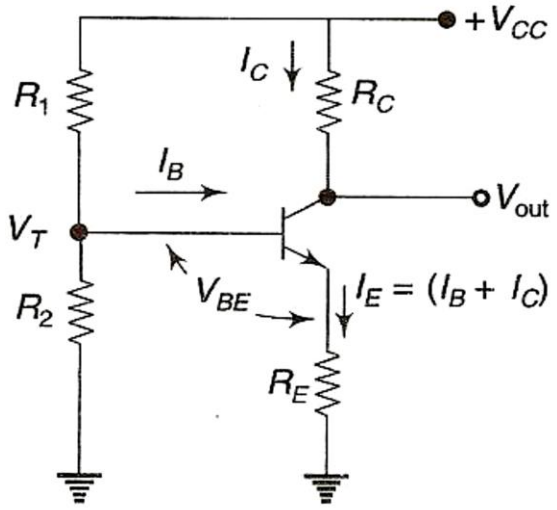


Fig.5.20: Circuit diagram of self-bias or voltage divider bias

- The resistors $R_1$and R_2 are in parallel. So, R_B= R_1// R_2. i.e. $R_B= \frac{R1R2}{R1+R2}$
- According to thevenin's theorem voltage across $R_2$is given by $V_T= \frac{Vcc\ R2}{R1+R2}$
- So, the self-bias circuit can be modified according to Thevinin's equivalent circuit is Thevenin voltage (V_T) in series with Resistance R_B.

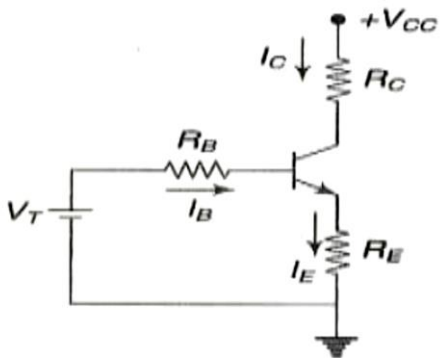


Fig.5.21: Thevenin's equivalent circuit diagram

- Apply loop equation for base circuit: $V_T = I_B R_B + V_{BE} + I_E R_E$
- Total current $I_E = I_B + I_C$. Substitute I_E in above equation, then it becomes

$$I_B = V_T - V_{BE} / (R_B + (1+\beta) R_E)$$

- Once I_B is known, the remaining quantities of the network V_E, V_C, and V_B can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Approximate Analysis :

- The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E.
- If *Ri* is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1.
- If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then I_1 &I_2 and R_1 and R_2 can be considered series elements.

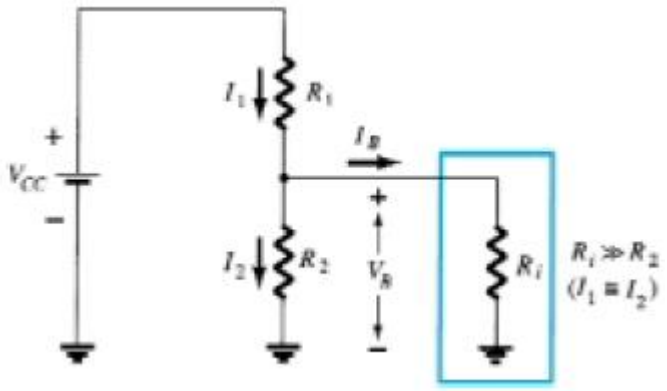


Fig.5.22: Partial-bias circuit for calculating the approximate base voltage V_B.

- Since $R_i=(1+\beta)R_E=R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$R_E >> 10R_2$$

- In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.
- **Saturation Level :** The collector saturation level or maximum collector current for a self bias design can be determined by

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

- **Load-Line Analysis:** The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

- Choosing I_C=0 mA gives

$$V_{CE} = V_{CC} \text{ at } I_C = 0 \text{ mA}$$

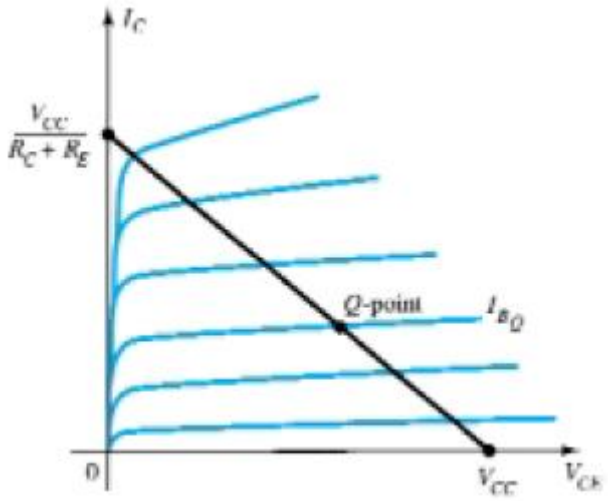


Fig.5.23: Load line for the emitter-bias configuration

- Different levels of I_{BQ} will, of course, move the *Q*-point up or down the load line can observe in Fig 5.24.

5.6 DC BIAS WITH VOLTAGE FEEDBACK

- An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 5.24.
- Although the *Q*-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations.

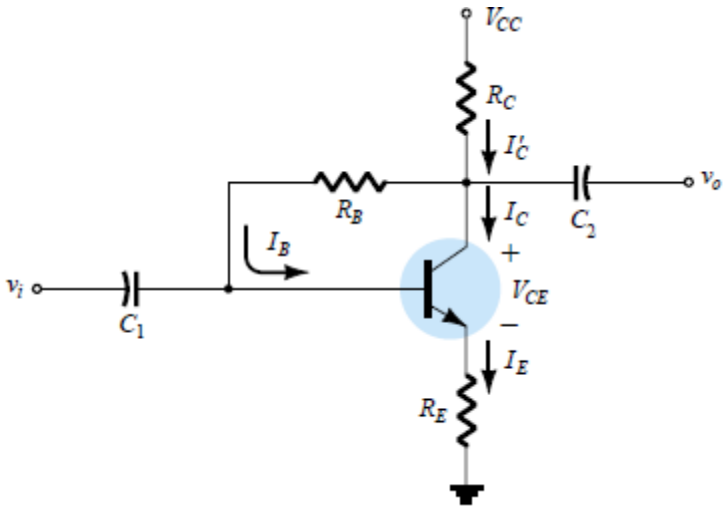


Fig.5.24: dc bias circuit with voltage feedback.

- **Base–Emitter Loop**: Fig 5.25 shows the base–emitter loop for the voltage feedback configuration.

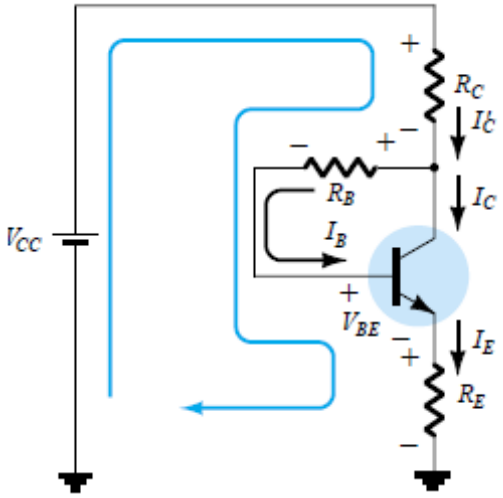


Fig.5.25: Base–emitter loop

- Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I'c = Ic + I_B$

- Substituting $I_C \approx I_C + I_B$ and $I_E = I_C$ will result in

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

- **Collector–Emitter Loop :** The collector–emitter loop for the network of Fig. 5.24 is provided in Fig. 5.26.

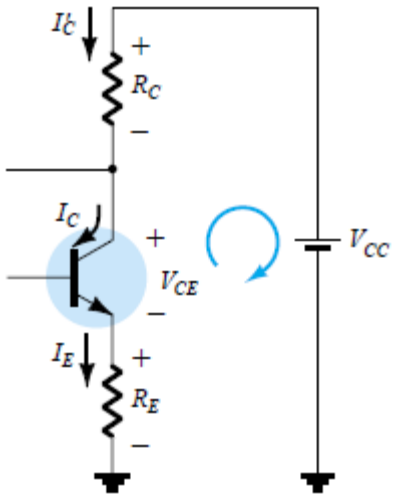


Fig.5.26: **Collector–emitter loop**

- Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$I_E R_E - V_{CE} - I_C R_C - V_{CC} = 0$$

Since $I'_C = I_C$ and $I_E = I_C$, we have

and $V_{CE} = V_{CC} - I_C(R_C + R_E)$

This is exactly as obtained for the emitter-bias and voltage-divider bias configurations

- **Saturation Conditions:** Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,
- **Load-Line Analysis :**Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. But the level of I_{BQ} will be defined by the chosen bias configuration.

5.7 BIAS STABILIZATION :

- For faithful amplification, the following conditions must be satisfied:
  - (i) Proper zero signal collector current I_C
  - (ii) Proper base-emitter voltage V_{BE}
  - (iii) Proper collector-emitter voltage V_{CE}

- The value of I_C and V_{CE} is expressed in terms of operating point or quiescent point Q. For faithful amplification, Q-point must be selected properly. The fulfillment of the above conditions is known as transistor biasing.
- While fixing the Q-point it has to be seen that the output of the amplifier is a proper sinusoidal waveform for sinusoidal input without distortion.
- If an amplifier is not biased properly, it can go into saturation or cut-off when an input signal is applied.
- By fixing the Q-point at different positions, we can observe the variation in collector current and collector-emitter voltage corresponding to a given variation of base current. If it enters into cut-off region, positive peak of the amplified ac signal will be clipped and if it enters into saturation, negative peak of the amplified ac signal will be clipped off.
- When the Q-point is located in the middle of the DC load line, sinusoidal waveform without distortion can be obtained at the output.
- Hence, values of different resistances and voltages must be selected in such a way that the Q-point should be:
  (i) in active region.
  (ii) on DC load line.
  (iii) selected in middle of the DC load line to avoid clipping of signals.
- **Factors affecting stability of Q –point :** The collector current I_C depends on reverse saturation current I_{CO}, base-emitter voltage V_{BE} and current gain β. These parameters are temperature dependent; i.e. as temperature changes, these parameters change. It results change in collector current I_C. Due to this, the Q-point will be changed. Hence, the Q-point has to be stabilized against temperature variation.

  I. **I_{CO}:** The collector current is given by $I_C=\beta I_B+ (\beta+ 1)I_{CO}$

  When a p-n junction is reverse biased, there is a small amount of current due to flow of minority carriers across the junction. Since minority carriers are thermally generated, reverse saturation current I_{CO} is extremely temperature dependent. The reverse saturation current I_{CO} doubles for every 10^oC rise in temperature. The flow of collector current produces heat at the collector junction. This increases the temperature; therefore reverse saturation current I_{CO} increases. Hence, collector current I_C again increases. This increase in I_C increases the temperature of collector junction which increases I_{CO} again. The effect is cumulative and at one stage I_C is so large which damages the transistor. Hence, the Q-point has to be stabilized against I_{CO} variation.

  II. **V_{BE}:** The base-emitter voltage V_{BE} decreases at the rate of 2.5 mV/^{o}C; i.e. the device starts operating at lower voltages. It results change in base current I_B. Since $I_C=\beta I_B$, collector current I_C changes. Hence, the Q-point has to be stabilized against V_{BE} variation.

  III. **β :** The transistor parameter β is temperature and device dependent .β increases with the increase in temperature. The value of β is different even for transistors of the same type. If the transistor is replaced by another transistor even of the same type, the value of β is different. It results change in collector current I_C.

As temperature changes, I_{CO}, V_{BE} and β change. Hence, collector current I_C changes with the change in temperature.

- **Stability Factors :** It is desirable and necessary to keep I_C constant with respect to variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under: The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} at constant β and V_{BE} is called **stability factor (S)**.

$$S = \frac{\Delta I_C}{\Delta I_{CO}}, \beta \& I_B \text{ Constant} \qquad \text{Or} \qquad S = \frac{dI_C}{dI_{co}}$$

Collector current Ic $= \beta I_B + (\beta+1) I_{CO}$ - (1)

Differencing eqn. (1) with repeat to Ic.

$$\frac{dI_c}{dI_c} = \frac{d\beta I_B}{dI_c} = \frac{d(\beta+1)I_{co}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_C} + (\beta+1)\frac{DI_{CO}}{dI_C}$$

$$1 - \beta \frac{dI_B}{dI_c} = \frac{\beta+1}{S}$$

$$\text{Or} \quad S = \frac{\beta+1}{1-\beta\left[\frac{dIB}{dIc}\right]}$$

- S should be as small as possible to have better stability.
- The rate of change of collector current I_C w.r.t. the V_{BE} at constant β and I_{CO} is called **stability factor (S^{I})**.

$$S' = \frac{dI_c}{dV_{BE}} \approx \frac{\Delta I_c}{\Delta V_{BE}}, Ico \& \beta \text{ constant}$$

- The rate of change of collector current I_C w.r.t. β at the constant V_{BE} and I_{CO} is called stability factor (S^{II}).

$$S'' = \frac{dI_c}{d\beta} \approx \frac{\Delta I_c}{\Delta\beta}, I_{co} \& V_{BE} \quad \text{constant}$$

- The larger the value of stability factor, the more sensitive is the circuit to variations in that parameter. The total change in collector current over a specified temperature range is obtained by expressing this change as the sum of individual changes due to three stability factors.

$$\Delta I_C = S\,\Delta I_{CO} + S'\,\Delta V_{BE} + S''\,\Delta\beta$$

- **Stability factor for fixed-bias configuration**: For the fixed-bias configuration, S=1+β. The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.
- **Stability factor for voltage-divider bias configuration :**

  Apply loop equation for base circuit of voltage divider bias network $V_T = I_BR_B+V_{BE}+I_ER_E$
  Total current $I_E=I_B+I_C$. Substitute I_E in above equation, then it becomes

$$V_T = I_BR_{th} +V_{BE}+ (I_B+I_C)R_E$$
$$V_T = I_BR_{th}+V_{BE}+I_BR_E +I_CR_E$$
$$V_T = I_B(R_{th}+ R_E)+V_{BE}+ I_CR_E$$
$$I_B(R_{th}+ R_E) = V_T-V_{BE} - I_CR_E$$

  Differentiating above equation w.r.to I_C , we will get

$$\frac{dIB}{dIC} = \frac{-RE}{RE+Rth}$$
$$S = \frac{1+\beta}{1-\beta\left(\frac{dIB}{dIC}\right)}$$
$$S= \frac{1+\beta}{1+\beta\left(\frac{RE}{RE+Rth}\right)}$$

  The stability factor of self-bias circuit or voltage divider bias is given by $S= \frac{1+\beta}{1+\beta\left(\frac{RE}{RE+Rth}\right)}$

- **Stability factor for feedback-bias configuration:**

  In this case

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C}$$

  Since the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

5.8 ENHANCEMENT-TYPE MOSFETs

- First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 5.27 For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \quad \text{……(5.4)}$$

- Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(on)}$) and its corresponding level of $V_{GS(on)}$, two points are defined immediately

as shown in Fig. 5.27.

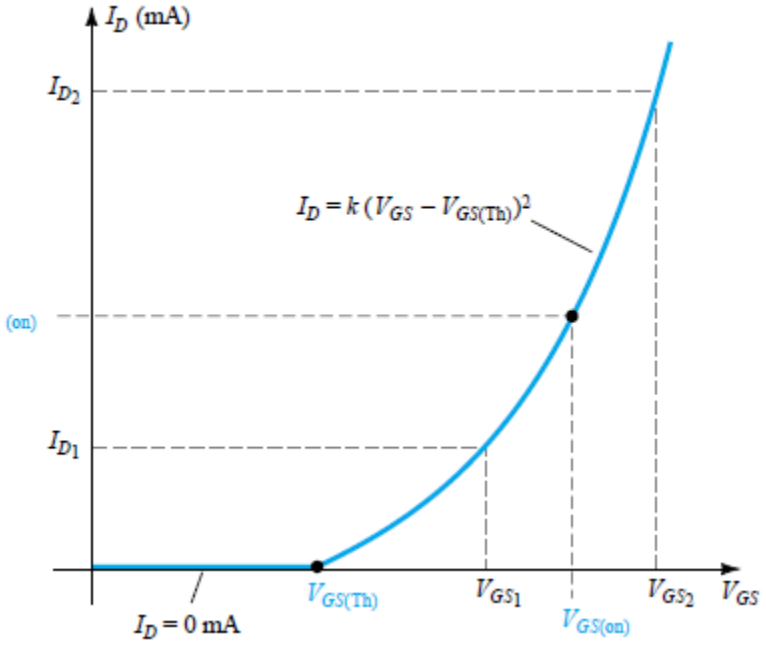


Fig.5.27: Transfer characteristics of an *n*-channel enhancement type MOSFET.

- To complete the curve, the constant k of Eq. (5.4) must be determined from the specification sheet data by substituting into Eq. (5.4) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$I_{D(on)} = k(V_{GS(on)} - V_{GS(Th)})^2$$

$$\boxed{k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}}$$

- Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(Th)}$ and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ will provide a sufficient number of points to plot Eq. (5.4) (note I_{D1} and I_{D2} on Fig.5.27).

5.8 Feedback Biasing Arrangement

- A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 5.28. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on."
- Since $I_G = 0$ mA and $V_{RG} = 0$ V, the dc equivalent network appears as shown in Fig. 5.28. A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

And $V_{DS} = V_{GS}$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following

$$V_{GS} = V_{DD} - I_D R_D$$

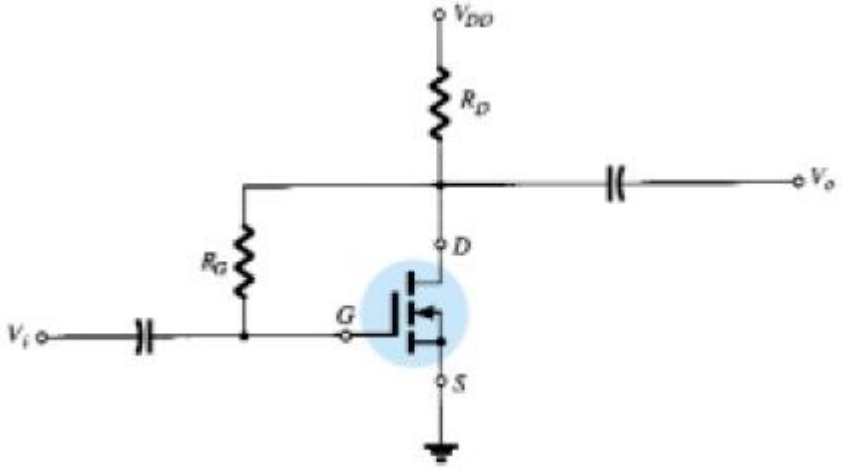


Fig.5.28: Feedback biasing arrangement

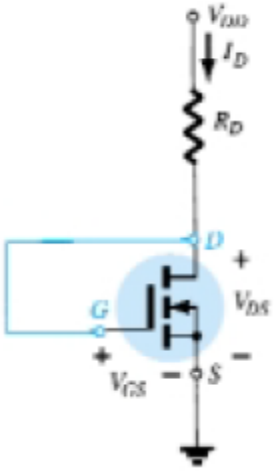


Fig.5.29: DC equivalent of the network of Fig. 5.28.

- This equation is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph.

  Substituting I_D = 0 mA into equation gives

$$V_{GS} = V_{DD}$$

- Substituting V_{GS}= 0 V into equation, we have I_D =*0mA*

$$I_D = V_{DD}/R_D$$

- The plots defined by equations appear in Fig. 5..38 with the resulting operating point.

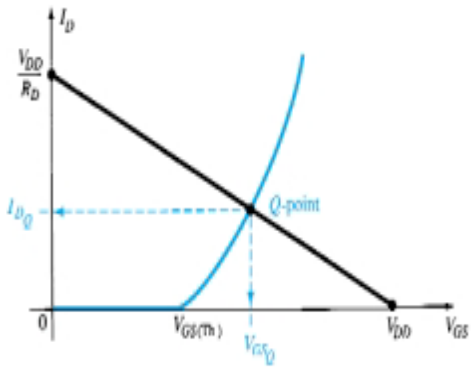


Fig.5.30:Determining the *Q* point for the network of Fig.5.29

5.9 Voltage-Divider Biasing Arrangement

- A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 5.31. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

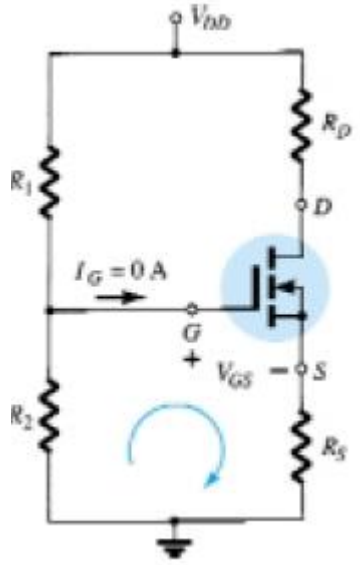


Fig.5.31 : Voltage-divider biasing arrangement for an *n* channel enhancement MOSFET.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

- Applying Kirchhoff's voltage law around the indicated loop of Fig. 5.31 will result in

$$+V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S$$

- For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

- Since the characteristics are a plot of I_D versus V_{GS} and above equation relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{DQ} and V_{GSQ} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

UNIT – 6

SMALL - SIGNAL MODELS OF MOSFET AND BJT

Objective: To familiarize with the operation, characteristics, applications and modeling of MOSFETs and BJT

Syllabus: MOSFET small-signal models, SPICE MOSFET models, BJT small-signal models, SPICE Ebers-Moll model and Gummel-Poon model.

Outcomes:

At the end of the unit, student will be able to

- familiarize with model and small signal operation of MOSFET circuits
- familiarize with model and small signal operation of BJT circuits

6.1 Small signal operation and models

- We learned up to that linear amplification can be obtained by biasing the MOSFET to operate in saturation region and by keeping the input signal small. Now turn our attention to exploring small signal operation in some detail.
- For small signal operation we are utilizing the common source amplifier circuit shown in below figure 6.1

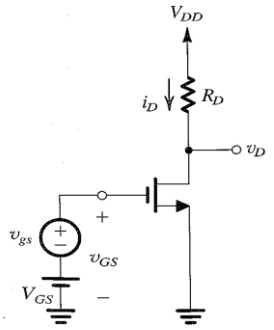


Fig. 6.1: Circuit to study the operation of MOSFET as a small signal amplifier.

- Here the MOS transistor biased by DC voltage V_{Gs} ,but is impractical arrangement but one this is simple for exploring small signal operation.

- The input signal v_{gs} is super imposed on the dc bias voltage V_{GS}. The output voltage is taken at the drain.

6.1.1 The DC Bias Point

- The DC current I_D can be found by setting the signal v_g, to zero : thus,

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

Where we have neglected channel – length modulation (i.e., we have assumed $\lambda = 0$).

- The DC voltage at the drain, VDS or simply VD(since S is grounded),will be

$$V_D = V_{DD} - R_D I_D$$

- To ensure saturation region operation, we must have

$$V_D > V_{GS} - V_t$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on V_D, V_D has to be sufficiently greater than $(V_{GS} - V_t)$ to allow for the required signal swing.

6.2.2 The Signal current in the Drain terminal

- Next, consider the situation with the input signal $v_{gs,}$ applied. The total instantaneous gate to source voltage will be

$$v_{GS} = V_{GS} + v_{gs}$$

Resulting in a total instantaneous drain current $i_{D,}$

$$\begin{aligned} i_D &= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 + k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \end{aligned}$$

- The first term on the right hand side of above equation can be recognized as the dc bias current I_D .The second term represents a current component that is directly proportional to the input signal V_{GS}. The third term is a current component that is proportional to the square of the signal. The last component is undesirable because it represents nonlinear distortion. To reduce the non-liner distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2}k_n'\frac{W}{L}v_{gs}^2 \ll k_n'\frac{W}{L}(V_{GS}-V_t)v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS}-V_t)$$

or, equivalently,

$$v_{gs} \ll 2V_{OV}$$

Where, V_{OV} is the overdrive voltage at which the transistor is operating.

- If this small signal condition is satisfied, we may neglect the last term and express i_D as

$$i_D \simeq I_D + i_d$$

Where,

$$i_d = k_n'\frac{W}{L}(V_{GS}-V_t)v_{gs}$$

The parameter that relates i_d and V_{GS} is the MOSFET trans-conductance (g_m)

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n'\frac{W}{L}(V_{GS}-V_t)$$

or in terms of overdrive voltage V_{OV},

$$g_m = k_n'\frac{W}{L}V_{OV}$$

Below Figure presents a graphical interpretation of the small – signal operation of the enhancement MOSFET amplifier.

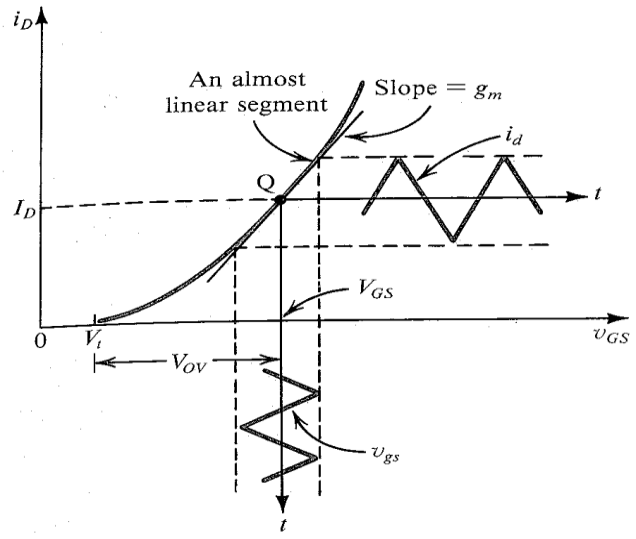


Fig.6.2: Small signal operation of the enhancement MOSFET amplifier

- Note that g_m is equal to the slope of the i_D - v_{GS} characteristics at the bias point.

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}}$$

6.1.3 The Voltage gain

- From Fig 1, we can express the total instantaneous drain voltage v_D as follows :

$$v_D = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_D = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as

$$v_D = V_D - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_d = -i_d R_D = -g_m v_{gs} R_D$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D$$

- The minus sign in above equation indicates that the output signal is 180^o out if phase with respect to the input signal V_{GS}.

- The below figure illustrates V_{GS} *and* V_D. The input signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$.For operation in the saturation region at all times, the minimum valueof V_D should not fall below the corresponding value of v_G by more than V_t..

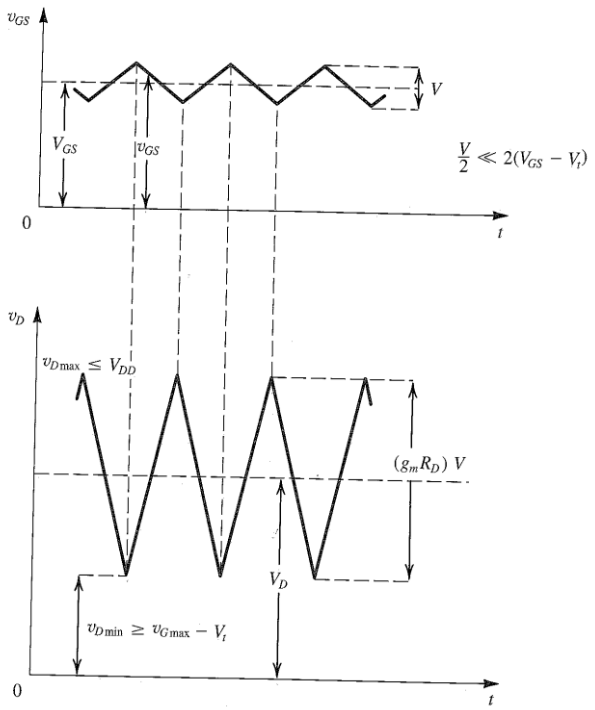


Fig. 6.3: Total Instantaneous voltages V_{GS} and V_D for the circuit

- The maximum value of V_D should be smaller than $V_{DD,}$ otherwise the FET will enter the cutoff region and the peaks of the output signal waveform will be clipped off.

6.1.4 Separating the DC Analysis and the signal Analysis

Under small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d, the total drain voltage $v_D = V_D + v_d$. Once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

6.1.5 Small – Signal Equivalent – Circuit Models

- From a signal point of view the FET behaves as a Voltage Controlled current source. It accepts a signal V_{GS} between gate and source and provides a current gm V_{GS}, at the drain terminal.

- The input resistance of this controlled source is very high – ideally infinite. The output resistance – i.e., resistance looking in to the drain – also is high.

- Putting all of this together, we get the circuit in Fig. 4.32 that represents the small signal model or small signal equivalent circuit.

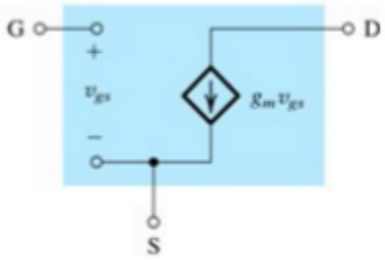


Fig. 6.4: Small signal model for the MOSFET neglecting the dependence of i_D on V_{DS} in saturation

- In the analysis of a MOSFET amplifier circuit, transistor can be replaced by the equivalent model. Ideal constant DC voltage sources are replaced by short circuit, and Ideal constant DC current sources are replaced by an open circuit in the small signal model.

- Another approach of the small signal model of amplifier is that assume the drain current in saturation is independent of the drain voltage. From MOSFET characteristics in saturation, we know that the drain current does in fact depend on V_{DS} in linear manner. Such linear relation was modeled by a finite resistance r_o between drain and source. we represent it as

$$r_o = \frac{|V_A|}{I_D}$$

- The current I_D is the value of the DC drain current without the channel –length modulation taken into account ; that is,

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

- Accuracy of the small signal model can be improved by including r_o in parallel with the controlled source.

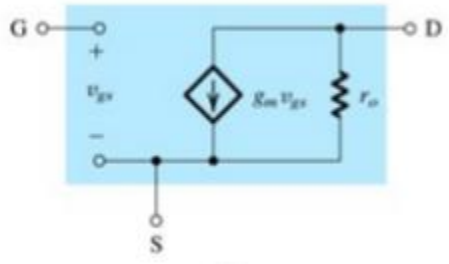


Fig.6.5: Small signal model for MOSFET including the effect of channel –length modulation.

- It is important to note that small signal model parameters g_m and r_o depend on the DC bias point of the MOSFET.

- MOSFET amplifier voltage gain expression

$$A_v = \frac{v_d}{v_{gs}} = -g_m(R_D // r_o)$$

- Thus finite output resistance r_o results in a reduction in the magnitude of voltage gain.

- All the above analysis performed on an NMOS transistor, apply equally well to PMOS device, except for using V_{GS}, V_t, V_{OV}, and V_A and replacing k_n' with k_p'.

6.1.6The Transconductance, g_m

- MOSFET transconductance is given by

$$g_m = k_n'(W/L)(V_{GS} - V_t) = k_n'(W/L)V_{OV}$$

- This relationship indicates that gm is proportional to transconductance parameters $kn' = \mu_n C_{ox}$ and to the W/L ratio of the MOS transistor; Hence to obtain large transconductance the device must be short and wide.

- Also g_m is proportional to overdrive voltage, $V_{ov}=V_{GS}$ - V_t. Increasing V_{GS} increases the g_m,but the device at larger V_{GS}has the disadvantage of reducing the allowable voltage signal swing at the drain.

- Another useful expression for g_m

$$g_m = \sqrt{2k_n'}\sqrt{W/L}\sqrt{I_D}$$

This expression shows that

1. g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $(W/L)^{1/2}$

- Another useful expression for g_m is

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}}$$

6.1.7 The T Equivalent Circuit Model

- It is possible to develop an alternate equivalent circuit model for the MOSFET. The development of such model is known as T model. Figure shows the equivalent circuit of MOSFET without r_o.

- In Figure 6.6(b) we have added a second g_mV_{GS} current source in series with the original controlled source. This addition of current source does not change the terminal currents.

- In Fig c The newly created circuit node, labeled as X , is joined to the gate terminal G. Observe that the gate current doesn't change(remains equal to zero)-thus this connection doesn't alter the terminal characteristics.

- We have a controlled voltage source g_mv_{gs} connected across its control voltage vgs. We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. Thus the value of resistance is $v_{gs}/g_mv_{gs} = 1/g_m$. This replacement is shown in figure d

- Figure d is the T model, observe that *ig* is still zero, $i_d = g_mv_{gs}$ and is=$v_{gs}/(1/g_m)$ =g_mv_{gs}, all same as the original model in Figure 6.6(a)

- Note that the resistance between gate and source, looking into the gate, is infinite. This observation useful in many applications.

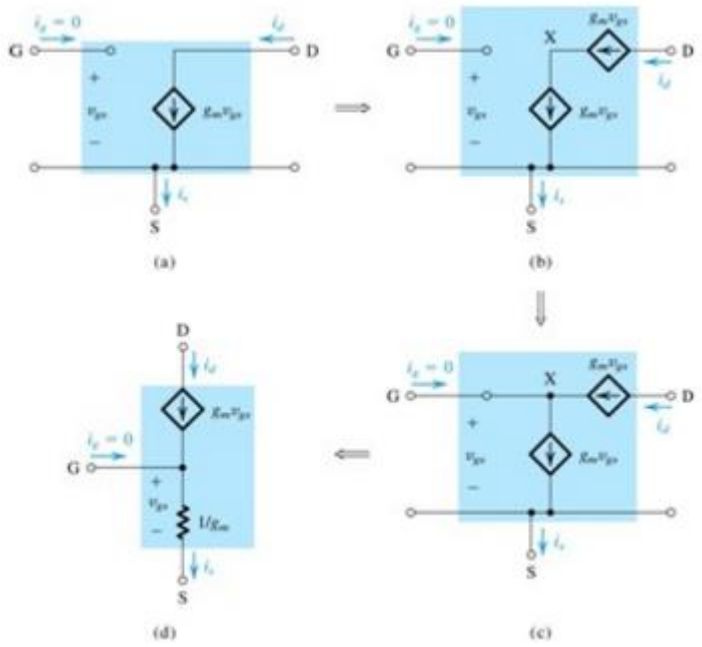


Fig.6.6: Development of the T equivalent – circuit model for the MOSFET. For simplicity, r_o has been omitted but can be added between D and S in the T model of (d).

- In T-model including resistance r_o between drain and source the circuit is modeled as follows.

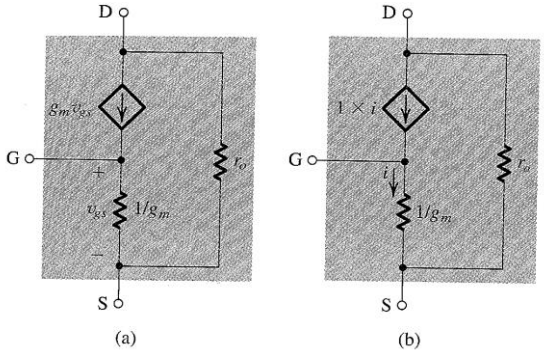


Fig 6.7: (a)The T model of the MOSFET augmented with the drain to source resistance r_o; (b) An alternative representation of the T model.

6.1.8 Modeling the Body Effect

- The body effect occurs in a MOSFET when the source is not tied to the substrate(which is always connected to the most negative power supply in the integrated circuit for n channel devices and to the most positive for p channel devices).
- Thus substrate(body) will be signal ground, but source is not.Since a signal voltage v_{bs} ddevelops between the body(B) and source(S).
- Since Substrate acts as back gate or second gate for MOSFET, the signal v_{BS} gives rise to a drain current component, which we shall write as $g_{mb}v_{bs}$.

  Where, g_{mb} is the Body Transconductance, defined as

$$g_{mb} \equiv \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{\substack{v_{GS}=\text{constant}\\ v_{DS}=\text{constant}}}$$

- Recalling that i_D depends on $\boldsymbol{v_{BS}}$ through the development of V_t on $V_{BS,}$ from that

$$g_{mb} = \chi g_m$$

  Where,

$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$

  Typically value of χ lies in the range 0.1 to 0.3.

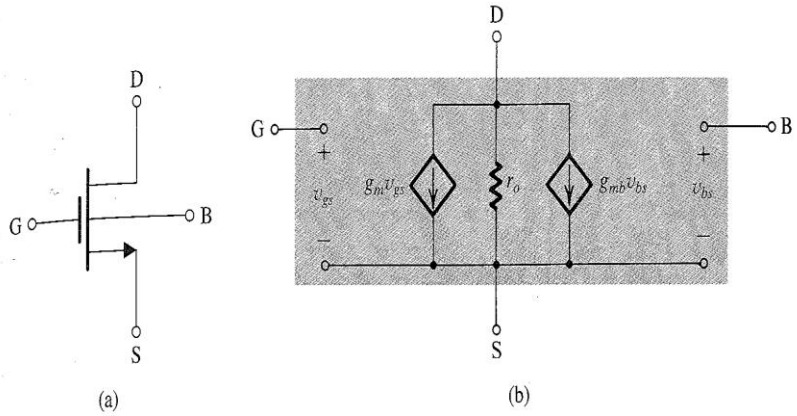


Fig. 6.8: Small signal equivalent circuit model of a MOSFET in which the source is not connected to the body

- Above Figure 4.36 shows the MOSFET model augmented to include the controlled source gmbvbs that models the body effect.This is the model to be used whenever the source is not connected to substrate.

- All the above analysis performed on an NMOS transistor, apply equally well to PMOS device, except for using V_{GS}, V_t, V_{OV}, V_A, V_{SB}, γ and λ replacing k_n' with k_p'.

6.2 MOSFET internal capacitances and high-frequency model

There are basically two types of internal capacitances in the MOSFET

(i)**The gate capacitive effect**: The gate electrode forms a parallel capacitor with the channel, with the oxide layer serving as the capacitor dielectric

(ii) **The source body and drain body depletion layer capacitances**: These are the capacitances of the reverse biased pn junction formed by n+ source region(also called source diffusion) and the p-type substrate and by the n+ drain region(the drain diffusion) and the substrate.

these two capacitive effect can be modelled by including capacitances in the MOSFET model between its four terminals, G,D,S and B. There will be five capacitances in total: C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db}, where the substrate indicate the location of the capacitance in the model

6.2.1 The Gate Capacitive Effect

i. when the MOSFET is operating in the triode region at small V_{DS} the channel will be uniform depth.the gate channel capacitance be WLC_{ox} and can be modeled by dividing it equally between source and drain ends. thus

$C_{gs} = C_{gd = 1/2}(WLC_{ox})$ (Triode region)

ii. when the MOSFET is operating in the saturation region

$C_{gs} = {}_{2/3}(WLC_{ox})$ and $C_{gd=0}$ (Saturation region)

iii when the MOSFET is operating in the cutoff region

$C_{gs} = C_{gd =} 0$ and $C_{gb =} WLC_{ox}$ (cut off)

iv There is an additional small capacitive component that should be added to C_{gs}, C_{gd} in all the preceding formulas. Thos capacitance that results from the fact that the source and drain diffusion extends slightly under the gate oxide. If the overlap length is denoted by L_{ov}. There is a overlap capacitance component is

$C_{ov} = W L_{ov} C_{ox}$

6.2.6 The junction capacitances

The Junction Capacitances :

The depletion-layer capacitances of the two reverse-biased junctions formed between each of the source and the drain diffusions and the body can b e determined using the formula developed in previous Section . Thus, for the source diffusion, we have the source body capacitance, *Csb*,

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

here Csb_0 is the value of *Csb* at zero body-source bias, *VSB* is the magnitude of the reverse bias voltage, and V_0 is the junction built-in voltage (0.6V to 0.8V). Similarly, for the drain diffusion, we have the drain-body capacitance *Cdb*,

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

6.3 The High-Frequency MOSFET Model:

The below figure shows the high frequency model of MOSFET by adding all the capacitances.

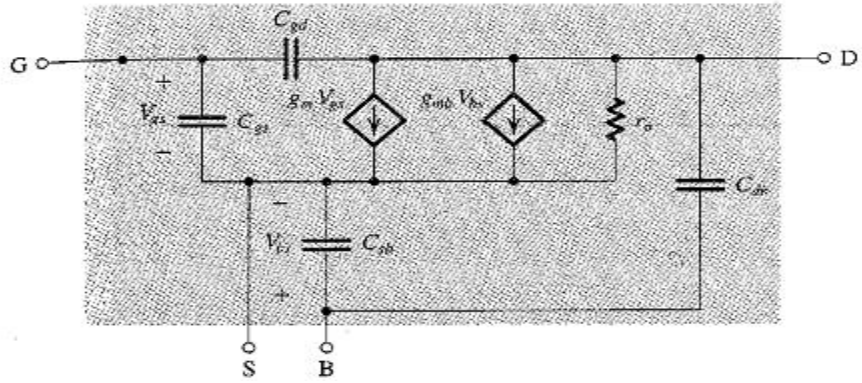


Figure 6.9 a: High-frequency equivalent circuit model for the MOSFET.

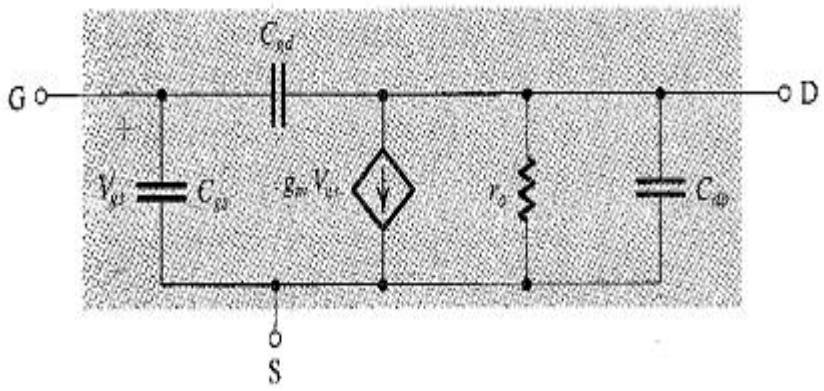


Figure 6.9 b: The equivalent circuit for the case in which the source is connected to the substrate (body),

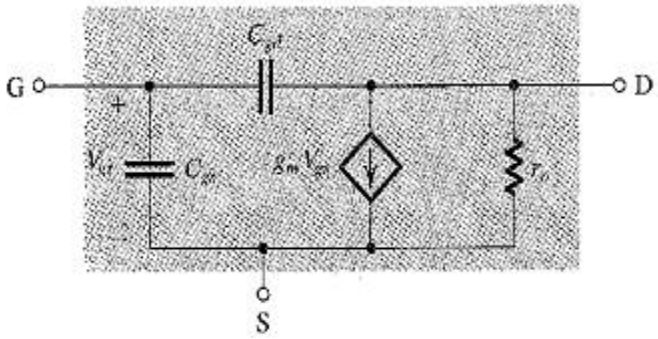


Figure 6.9 c: The equivalent circuit model of (b) with *Cdb* neglected (to simplify analysis).

6.4 The MOSFET Unity-Gain Frequency *(f_T):*

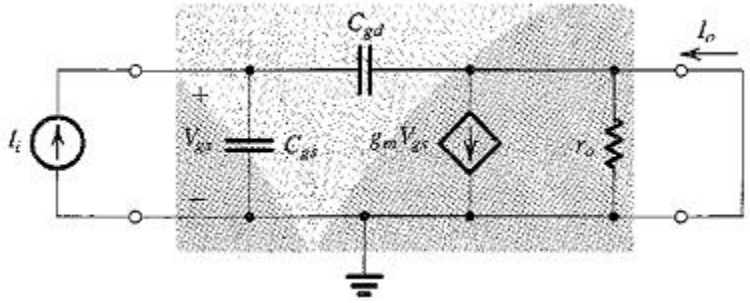


Figure 6.10: Circuit for determining the short-circuit current gain $I_o/1_i$.

A figure of merit for the high-frequency operation of the MOSFET as an amplifier is the unity-gain frequency, f_T. This is defined as the frequency at which the short-circuit current gain

of the common-source configuration becomes unity. The above figure shows the MOSFET hybrid ∏- model with the source as the common terminal between the input and output ports. To determine the short-circuit current gain, the input is fed with a current-source signal I_i• and the output terminals are short-circuited. It is easy to see that the current in the short circuit is given by

$$I_o = g_m V_{gs} - sC_{gd}V_{gs}$$

let us assume C_{gd} is a very small value and it can be neglected

w e can express *Vgs* in terms of the input current I_i as

$$V_{gs} = I_i / s(C_{gs} + C_{gd})$$

By the above two equations we can get the short circuit current gain as

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

For physical frequencies *S=JW,* it can be seen that the magnitude of the current gain becomes unity at the frequency

$$\omega_T = g_m/(C_{gs} + C_{gd})$$

Thus the unity-gain frequency f_T is given as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Hence f_T is proportional to *gm* and inversely proportional to the FET internal capacitances.

6.6 Small signal operations and models of BJT

- Now take a closer look at the small signal operation of the transistor .Towards that consider conceptual circuit shown in below fig. 6.11. Here base emitter junction is forward biased by a DC voltage V_{BE}. The reverse bias of collector base junction by V_{CC} through a resistor Rc. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE}.

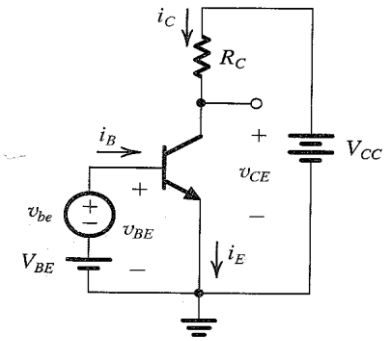


Fig. 6.11: Conceptual circuit to illustrate the operation of the transistor as an amplifier.

- First make the DC bias condition by setting the signal v_{BE} to zero and the circuit reduces to that in the following figure 5.28.

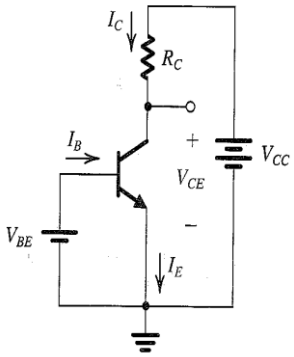


Fig. 6.12: The circuit with the signal source v_{be} eliminated for dc(bias) analysis.

- we can write the following relationships for the DC currents and voltages :

$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

$$V_{CE} = V_{CC} - I_C R_C$$

- Obviously for a active mode operation, Vc should be greater than (V_B – 0.4) by an amount that allows for a reasonable signal swing at the collector.

6.6.1 The Collector Current and the Trans conductance

- If a signal v_{be} is applied as shown in Fig. 6.12 ,The total instantaneous base emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$
$$= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$$

Use Ic equation

$$i_C = I_C e^{v_{be}/V_T}$$

Now if $v_{be} << V_T$, we may approximate

$$i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right)$$

This approximation is valid only for v_{be} less than approximately 10mv,is referred to as the small signal approximation. Under this approximation the total collector current can be written as

$$i_C = I_C + \frac{I_C}{V_T} v_{be}$$

Thus the collector current is composed of the dc bias value Ic and a signal component ic,

$$i_c = \frac{I_C}{V_T} v_{be}$$

This equation relates the signal current in the collector to the corresponding base – emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be}$$

Where g_m is called the Trans conductance, and it is given by

$$g_m = \frac{I_C}{V_T}$$

We observe that the trans conductance of the BJT is directly proportional to the collector bias current Ic.

- A graphical interpretation for g_m is given in figure 5.30, Where it is shown that g_m is equal to the slope of the i_c - v_{BE} characteristic curve at i_c = Ic. Thus

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C}$$

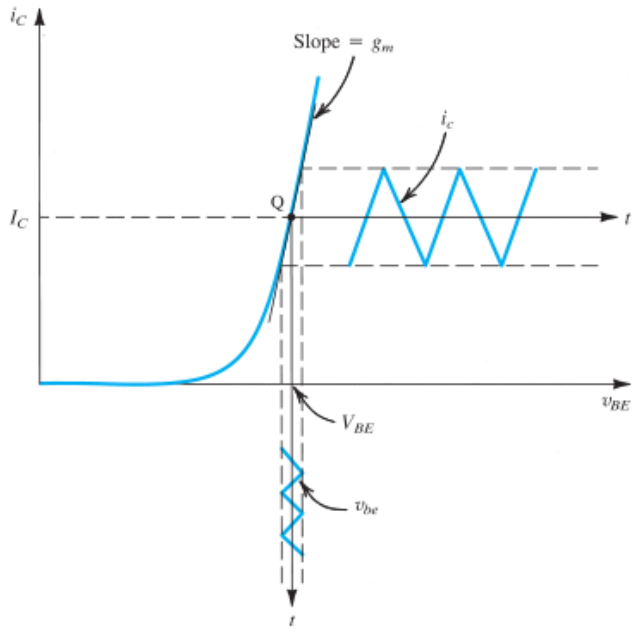


Fig. 6.13: Linear operation of the transistor under small signal condition

- The small signal approximation implies keeping the signal amplitude sufficiently small so that operation is restricted to an almost linear segment of the i_c - v_{BE} exponential curve. Increasing the signal amplitude will result in the collector current having components nonlinearly related to v_{be}.
- For small signals ($v_{be} << V_T$) the transistor behaves as a voltage controlled current source. The input port of this controlled source is between base and emitter, and the output port is between collector and emitter. The trans conductance of the controlled source g_m and the output resistance is infinite.
- The collector voltage has no effect on the collector current in the active mode.
- Practical BJT's have finite output resistance because of the Early effect. The effect of output resistance on amplifier performance will be considered later.

6.6.2 The base current and the Input Resistance at the Base

- To determine the resistance by v_{be}, we first evaluate the total base current i_B

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T} v_{be}$$

Thus,

$$i_B = I_B + i_b$$

Where i_B is equal to Ic /β and the signal component i_b is given by

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Substituting for Ic/V_T by g_m gives

$$i_b = \frac{g_m}{\beta}v_{be}$$

- The small-signal resistance between base and emitter, looking into the base,is donated by r_π and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b}$$

$$r_\pi = \frac{\beta}{g_m}$$

- Thus r_π is directly dependent on β and is inversely proportional to the bias current Ic. Substitute g_m and replacing Ic/β by I_B gives an alternative expression for r_π,

$$r_\pi = \frac{V_T}{I_B}$$

6.6.3 The Emitter current and the Input Resistance at the Emitter

- The total current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} \rightarrow i_E = I_E + i_e$$

- Where I_E is equal to I_c /α and the signal current i_e is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T}v_{be} = \frac{I_E}{V_T}v_{be}$$

- If we denote the small signal resistance between base and emitter, looking into the emitter, by r_e, it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e}$$

- We find that r_e called the emitter resistance, is given by

$$r_e = \frac{V_T}{I_E}$$

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m}$$

- The relationship between r_π and r_e can be found by combining their respective definitions and is given as

$$v_{be} = i_b r_\pi = i_e r_e$$

Thus

$$r_\pi = (i_e / i_b) r_e$$

Which yields,

$$r_\pi = (\beta + 1) r_e$$

6.6.4 Voltage Gain

- In the preceding section we have established only that the transistor senses the base emitter signal v_{be} and causes a proportional current $g_m v_{be}$ to flow in the collector lead at a high(ideally infinite) impedance level. In this way transistor is acting as a voltage – controlled current source.
- To obtain an output voltage signal, we may force this current to flow through a resistor. Then the total collector voltage v_c will be

$$\begin{aligned} v_{CE} &= V_{CC} - i_C R_C \\ &= V_{CC} - (I_C + i_c) R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C \\ &= V_{CE} - i_c R_C \end{aligned}$$

- Here the quantity V_c is the dc bias voltage at the collector, and the signal voltage is given by

$$v_{ce} = -i_c R_C = -g_m v_{be} R_C$$

$$= (-g_m R_C) v_{be}$$

- Thus the voltage gain of this amplifier A_v is

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C$$

- Here again we note that because g_m is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made.

  Substitute g_m in Av

$$A_v = -\frac{I_C R_C}{V_T}$$

6.6.6 The Hybrid – π Model

An equivalent circuit model for the BJT is shown in below fig

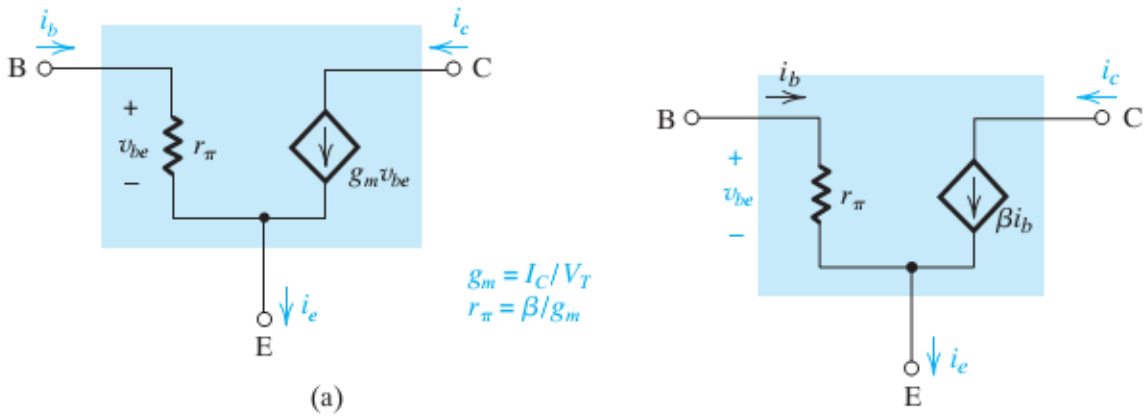


Fig. 6.14: Two slightly different versions of the simplified hybrid –π model for the small signal operation of the BJT. The equivalent circuit in (a) represents the BJT as a voltage controlled current source (a transconductance amplifier), and that in (b) represents the BJT as a current controlled current source (a current amplifier).

- Model (a) represents the BJT as a voltage controlled current source and explicitly includes the input resistance looking into the base r_π. The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be}/r_\pi$.
- At the emitter node we have

$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi}(1 + \beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right) \\ &= v_{be}/r_e \end{aligned}$$

- A slightly different circuit model(b) can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b (current controlled current source) as follows:

$$\begin{aligned} g_m v_{be} &= g_m(i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

- The two models (a & b) are the simplified hybrid –π model for the small signal operation for the BJT. The model parameters g_m, r_π depend on the value of the DC bias current Ic.
- Finally, although the models have been developed for an NPN transistor, they apply equally well to a PNP transistor with no change of polarities.

6.6.7 The T Model

- Although hybrid –π model can be used to carry out small signal analysis of all transistor circuits, there are situations in which alternative model shown in below fig, is much more convenient, is called as T model.

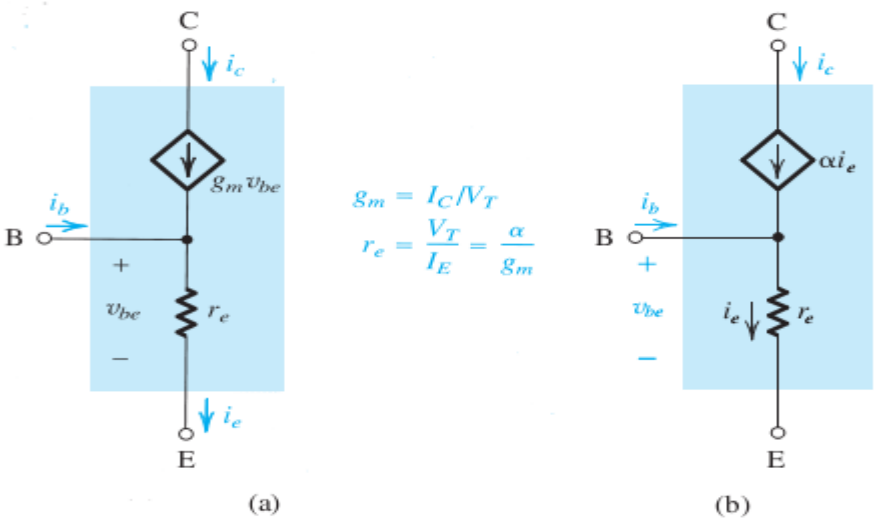


Fig. 6.15: Two slightly different versions of what is known as the T model of the BJT. The circuit in (a) is a voltage controlled current source representation and that in (b) is a current controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid –π model.

- The two versions of T-model shown in above figure. Fig. (a) represents the BJT as a voltage controlled current source with the control voltage being v_{be}. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown.
- From fig(a) we see clearly that the model yields the correct expression for i_c and i_b. For i_b we note that at the base node we have

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

$$= \frac{v_{be}}{r_e}(1 - \alpha) = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta + 1}\right)$$

$$= \frac{v_{be}}{(\beta + 1) r_e} = \frac{v_{be}}{r_\pi}$$

- If in the model of Fig (a) the current of the controlled source is expressed in terms of the emitter current as follows :

$$g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$

- We obtain alternative T-model shown in Fig (b). Here the BJT is represented as a current –controlled current source but with the control signal being i_e

6.6.10 Augmenting the Small signal Models to Account for the Early Effect

- The Early effect disscussed in previous,causes the collector current to depend not only on v_{BE} but also on v_{CE}.
- The dependence on v_{CE} can be modeled by assigning a finite output resistance to the current controlled current source in the hybrid – π model,as shown in below Fig. 5.34

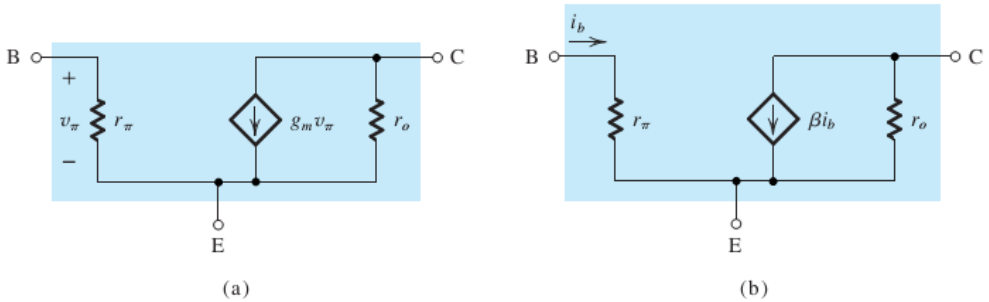


Fig. 6.16:Hybrid –π small signal model in it's two versions,with r_o included.

- The output resistance r_o was defined and is given by $r_o = V_A/I_C$,Where V_A is Early voltage.Note that in the models we renamed v_{be} and v_π.
- The effect of r_o on the operation of the amplifier is , r_o Simply appears in parallel with R_c.Thus ,if we include r_o in the equivalent circuit the output voltage becomes

$$v_o = -g_m v_{be}(R_C \parallel r_o)$$

- Thus the gain will be somewhat reduced. Obviously if $r_o >> Rc$ the reduction in gain will be negligable.and one can ignore the effect of r_o.In general ,in such configuration $r_o$can be neglected if it is greater than 10Rc.If emitter is not connected to the ground,including r_o in the model gives complicated analysis.

6.7 The BJT Internal Capacitances and High Frequency Model

The high frequency response of BJT amplifiers rolls off due to short circuiting effect of internal capacitances. These internal capacitances are resulting from charge- storage effects.

The High frequency Hybrid- π model is shown as below.

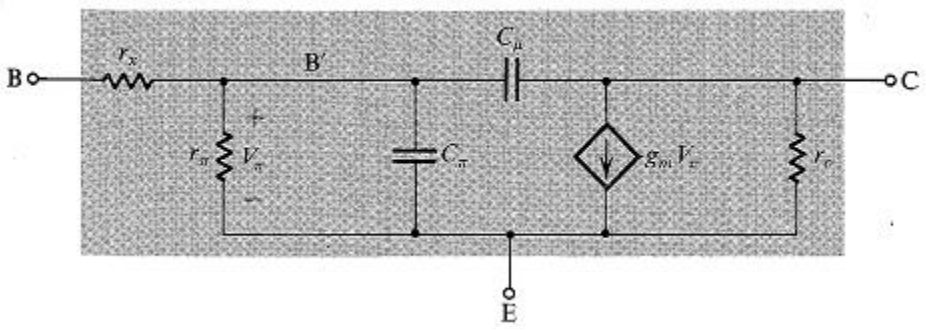


Fig 6.17. The High- Frequency Hybrid - π model

r_x : Base Spreading Resistance :

It is the resistance between the external base terminal B and internal node B' (also called as implicit node, bulk node). Its typical value is 100Ω. negligible at low frequencies but effective at high frequencies.

r_Π: It is the resistnace looking into the base terminal.

typical value is 1KΩ.

There are two sources of internal capacitances effect

1. Base- Emitter Capacitance Cπ

2. Collector –Base Junction Capacitance Cμ

1. Base- Emitter Capacitance Cπ :

Cπ is the sum of two capacitances .Cde Emitter- Base Diffusion Capacitance

Cje Emitter – Base Junction Capacitance.

$$C\pi = Cde + Cje$$

i) Cde Emitter- Base Diffusion Capacitance: It is called as Base – Charging or Diffusion Capacitance Cde.

It is due to minority carrier storage in the base region when the transistor is operating in the active or satuaration mode. i.e when Emitter- Base Junction (EBJ) is forward biased.

$Cde = dQ/dv_{BE}$

considering , an npn transistor in active region..

$$i_C = I_S e^{v_{BE}/V_T} \quad \text{.....(1)}$$

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

$$Q_n = \frac{A_E q W n_i^2}{2N_A} e^{v_{BE}/V_T} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

Using 1, 2, 3

$$Q_n = \frac{W^2}{2D_n} i_C = \tau_F i_C$$

where, $$\tau_F = \frac{W^2}{2D_n}$$

τ_F is known as the forward base- transit time. It represents the average time a charge carrier (electron) spends in crossing the base.

$$C_{de} \equiv \frac{dQ_n}{dv_{BE}}$$

$$= \tau_F \frac{di_C}{dv_{BE}}$$

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{V_T}$$

ii :Cje :: Base – Emitter Junction Capacitance

$$C_{je} = \frac{C_{je0}}{\left(1 - \frac{V_{BE}}{V_{0e}}\right)^m}$$

Where, Cje0 is the value of Cjeat VBE = 0V.

V_{0e} is the EBJ built in voltage (0.7 – 0.9 V)

m = grading coefficient , typically ½.

For a forward biased EBJ in the active mode, Cje = 2 Cje0

Typical value of Cπ is 100pF.

2. The Collector – Base Junction Capacitance Cμ

This is the capacitance of the reverse biased Collector – Base Junction (CBJ) .

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}$$

where Cμ0 is the value of Cμ at VCB = 0V.

Voc is the CBJ built in voltage (typically 0.75 V)

m is grading coeffiecient = 1/2 to 1/3 .

Typical value of Cμ= 3pF.

Unity Gain Frequency (F_T)

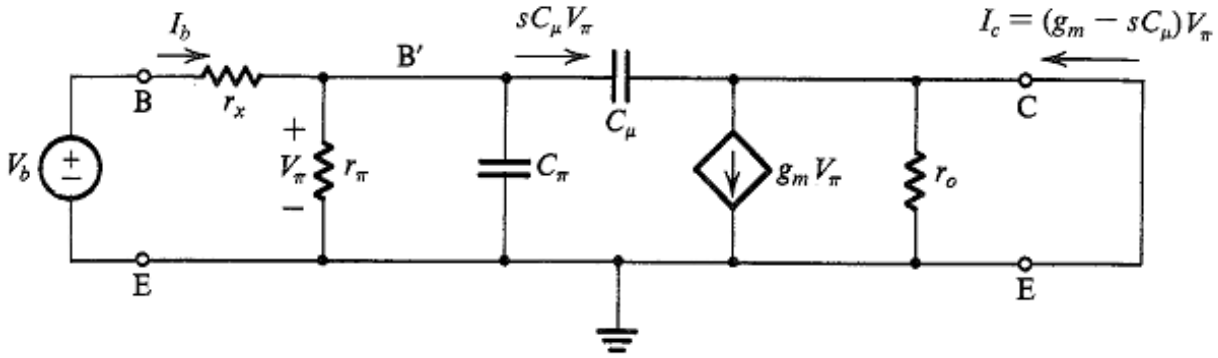


Fig.6.18 The Circuit for deriving an expression for Short Circuit current gain $h_{fe}(s)$ = Ic/ Ib.

$$I_c = (g_m - sC_\mu)V_\pi \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V_\pi = I_b(r_\pi // C_\pi // C_\mu) = \frac{I_b}{1/r_\pi + sC_\pi + sC_\mu} \quad \ldots\ldots\ldots\ldots(2)$$

$$h_{fe} \equiv \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{1/r_\pi + s(C_\pi + C_\mu)} \quad \ldots\ldots\ldots\ldots\ldots\ldots..(3)$$

Since,

$$g_m \gg \omega C_\mu;$$

$$h_{fe} \simeq \frac{g_m r_\pi}{1 + s(C_\pi + C_\mu) r_\pi}$$

$$h_{fe} = \frac{\beta_0}{1 + s(C_\pi + C_\mu) r_\pi}$$

Where β_0 is the low frequency value of β

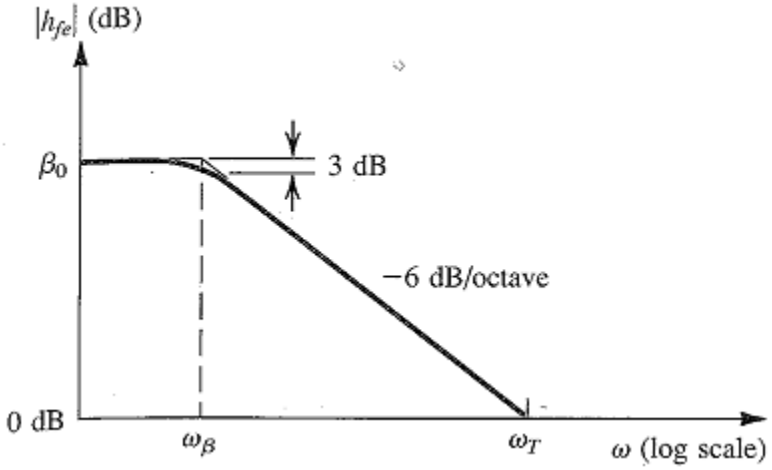


Fig. 6.19 Frequency Response of h_{fe}

f_β is the 3-dB frequency

$$\omega_\beta = \frac{1}{(C_\pi + C_\mu) r_\pi}$$

The unity gain frequency is given by

$$\omega_T = \beta_0 \omega_\beta$$

Thus

$$\omega_T = \frac{g_m}{C_\pi + C_\mu}$$

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

Assignment-Cum-Tutorial Questions

A. Questions testing the remembering / understanding level of students

I) Objective Questions

1. MOSFET can be used as _____
2. When the gate to source voltage is less than the threshold voltage, it will be operated in _____ region.
3. The condition required for MOSFET to operate in saturation region is [ ]

   a) $V_{DS} \geq (V_{GS} - V_t)$ b) $V_{DS} = V_t$ c) $V_{DS} \geq (V_{GS} - V_t)$ d) $V_{DS} = V_{GS}$
4. MOSFET can be used as an amplifier in which of the following operating regions.[ ]

   a) Triode region b) Cut-off region c) Saturation region d) both (a) and (c)
5. In a MOSFET operating in saturation, the channel length modulation effect causes [ ]

   a) increase in gate-to-source capacitance b) decrease in trans conductance

   c) decrease in unit gain cutoff frequency d) decrease in output resistance
6. What is sub-threshold conduction in MOSFET?
7. MOSFET uses the electric field of [ ]

   a) gate capacitance to control the channel current

   b) barrier potential of p-n junction to control the channel current

   c) both a and b

   d) none of these

8. In a MOSFET, the polarity of the inversion layer is the same as that of the [ ]
   a) charge on the gate electrode
   b) minority carriers in the drain
   c) majority carries in the substrate
   d) majority carries in the source
9. The drain current of MOSFET in saturation region is given by $I_D = K(V_{GS} - V_T)^2$ where, K is a constant. The magnitude of trans conductance is _____ [ ]
   a) $K (V_{GS} - V_T)^2 / V_{DS}$ b) $2K (V_{GS} - V_T)$ c) $I_D / (V_{GS} – V_{DS})$ d) $K (V_{GS} - V_T)^2 / V_{GS}$
10. For an n – channel enhancement type MOSFET, if the source is connected at a higher potential than that of bulk (i.e., $V_{SB}>0$), the threshold voltage V_T of the MOSFET will [ ]
    a) remain unchanged b) decreases c) change polarity d) increases
11. What is an advantage of MOS transistors in integrated circuits? [ ]
    a) Fast switching b) less capacitance
    c) higher component density & lower cost d) lower resistance
12. Draw the small – signal equivalent circuit of an n – channel MOSFET when it is operated in saturation region.
13. Draw the circuit symbols of p – channel MOSFETs.
14. Why MOSFET is called IGFET?
15. With the E-MOSFET, when gate input voltage is zero, drain current is .....
16. Draw the small signal equivalent circuit model including r_o for the MOSFET
17. Define gm, Av, and μ in MOSFET
18. Give the 3 useful expressions for g_m
19. Draw the T-equivalent circuit model for the MOSFET
20. Draw the Large signal equivalent circuit model of the npn BJT operating in reverse active mode.
21. Collector current Ic is directly proportional to gm (True/False)
22. What is Trans conductance, Voltage gain of BJT?
23. Draw the hybrid –π model of BJT.
24. Draw the T-equivalent circuit model for the BJT

II) Descriptive Questions

1. What is small signal operation? Draw the Small signal equivalent circuit models for the MOSFET?
2. Discuss Small signal model of MOSFET concepts about a) DC bias point b) Signal current in Drain terminal c) Transconductance and d) Voltage gain
3. Develop T Equivalent model for MOSFET.
4. Explain Body effect and Model the body effect in MOSFET.
5. Explain how the BJT acts as an amplifier with graphical analysis.

6. Explain small signal operation & Draw the equivalent circuit models for the BJT?
7. Discuss the Small signal operation concepts about a) Trans conductance, b) Voltage gain and c) input Resistance.
8. Discuss the internal capacitances of BJT
9. Discuss about the BJT High frequency model
10. Discuss the internal capacitances of MOSFET
11. Discuss about the MOSFET High frequency model

B. Question testing the ability of students in applying the concepts.

I) Objective Questions

1. When V_{SS} of a MOSFET with a threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1mA. Neglecting channel length modulation effect and assuming that the MOSFET is operating in saturation, what will be the drain current for an applied V_{GS} of 1400 mV?
2. For an n-channel MOSFET and its transfer curve shown in the Fig. P4.1, Find the threshold voltage and region of operation.

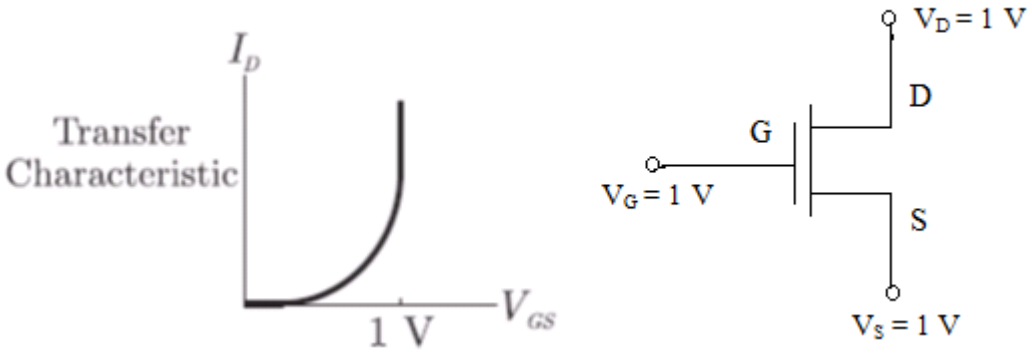
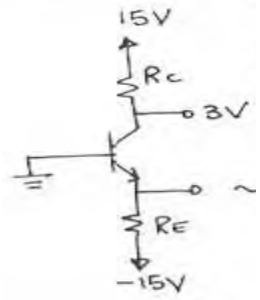


Fig.P4.1

3. With the knowledge that $\mu_p = 0.4\mu_n$, what must be the relative width of n-channel and p-channel devices if they are to have equal drain currents when operated in the saturation mode with overdrive voltages of the same magnitude?
4. For an NMOS transistor, for which $V_t = 0.8$ V, v_{GS} in the range of 1.5 V to 4 V, what is the largest value of v_{DS} for which the channel remains continuous?
5. For a particular IC-fabrication process, the transconductance parameter $k'_n = 50\ \mu A/V^2$, and $V_t = 1$ V. In in which $v_{GS} = v_{DS}$ = Vsupply =-5 V, a drain current of 0.8 mA is required of a device of minimum length of 2 μm. What value of channel width must the design use?
6. A p-channel transistor operates in saturation with its source voltage 3V lower than its substrate. For $\gamma = 0.5\ V^{1/2}$, $2\Phi_f = 0.75$ V, and $V_{t0} = -0.7$ V, find V_t.
7. With a 30V of V_{DD}, and 8KΩ drain resistor, what is the E-MOSFET Q point voltage, with $I_D = 3$ mA?
8. In a particular BJT, the base current is 7.5 μA, and the collector current is 400μA.Find β, α for this device.
9. An NPN transistor of a type whose β is specified to range from 60 - 300 is connected in a circuit with emitter grounded, collector at +9v and a current of 50 μA injected into the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor?
10. Design the circuit given below to provide β=100, Vc=+3V and Ic=5mA .

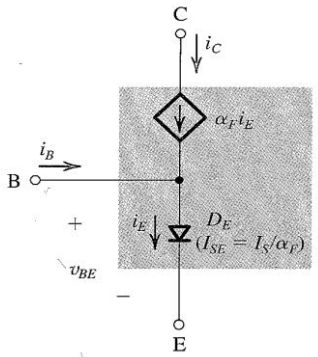


11. The current I_{CBO} of a small transistor is measured to be 20nA at 25° C. If the temperature of the device is raised to 85° C, What do you expect I_{CBO} to become?
12. A BJT whose emitter current is fixed at 1 mA has a base – emitter voltage of 0.69 V at 25° C. What base –emitter voltage would you expect at 0° C? At 100° C?
13. For a BJT having an Early voltage of 200 V, what is its output resistance at 1mA? At 100µA

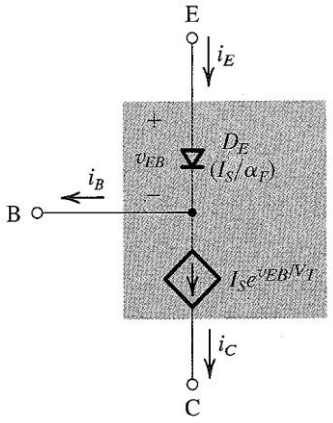
II) Problems

1. An n-channel device has k' = 50 µA/V^2, V_t = 0.8 V, and W/L = 20. The device is to operate as a switch for small v_{DS}, utilizing a control voltage v_{GS} in the range 0 V to 5 V. Find the switch closure resistance, r_{DS}, and closure voltage, V_{DS}, obtained when v_{GS} = 5 V and i_D = 1 mA. Recalling that μ_p= 0.4 μ_n, what must W/L be for a p-channel device that provides the same performance as the n-channel device in this application?
2. Consider a CMOS process for which $\boldsymbol{L_{min}}$= 0.8 µm, $\boldsymbol{t_{ox}}$ =15 nm, μ_n = 550 cm^2/V- s, and $\boldsymbol{V_t}$= 0.7 V. (a) Find ***Cox*** and ***k'n.*** (b) For an NMOS transistor with ***W/L*** = 16 µm/0.8 µm, calculate the values of ***Vov,*** $\boldsymbol{V_{GS}}$, and $\boldsymbol{V_{DS}}$ ***min*** needed to operate the transistor in the saturation region with a dc current I_D = 100 µA. (c) For the device in (b), find the value of ***Vov*** and $\boldsymbol{V_{GS}}$ required to cause the device to operate as a 1000 Ω resistor for very small $\boldsymbol{v_{DS}}$.
3. Consider an n-channel MOSFET with $\boldsymbol{t_{ox}}$= 20 µm, μ_n =650 cm^2/V- s, $\boldsymbol{V_t}$ = 0.8 V, and ***W/L*** = 10. Find the drain current in the following cases:
   (a) $\boldsymbol{v_{GS}}$ = 5V and $\boldsymbol{v_{DS}}$ = 1 V
   (b) $\boldsymbol{v_{GS}}$ = 2 V and $\boldsymbol{v_{DS}}$ = 1.2V
   (c) $\boldsymbol{v_{GS}}$= 5 V and $\boldsymbol{v_{DS}}$= 0.2 V
   (d) $\boldsymbol{v_{GS}}$ = $\boldsymbol{v_{DS}}$ = 5V

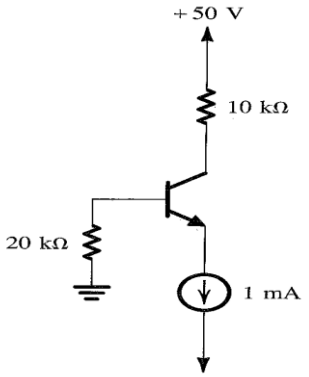
4. A particular enhancement MOSFET for which V_t =1 V and $k'_n(W/L)$ = 0.1 mA/V^2 is to be operated in the saturation region. If i_D is to be 0.2 mA, find the required V_{GS} and the minimum required v_{DS}. Repeat for i_D = 0.8 mA.
5. A particular n-channel enhancement MOSFET is measured to have a drain current of 4 mA at $V_{GS} = V_{DS}$= 5 V and of 1 mA at $V_{GS} = V_{DS}$= 3 V. What are the values of $k'_n(W/L)$ and V_t for this device?
6. A CE amplifier employing an NPN transistor has load resistor R_C connected between collector and Vcc supply of +16V. For biasing a resistor R_1 is connected between collector and base, resistor R_2=30KΩ is connected between emitter and ground. Draw the circuit diagram. Calculate the values of R_1 and R_C and the stability factor S if V_{BE}=0.2V, I_E=2mA, α_0=0.985 and V_{CE}=6V.
7. For a particular npn transistor operating at a v_{BE} of 670 mV and I_c = 3 mA, the i_C - v_{CE} characteristic has a slope of 3 x 10^{-5} mhos. To what value of output resistance does this correspond? What is the value of Early voltage for this transistor? For operation at 30 mA, what would the output resistance become?
8. Two transistors, fabricated with the same technology but having different junction areas, when operated at a base –emitter voltage of 0.72, have collector currents of 0.2 mA and 12mA.Find Is for each device. What are the relative junction areas?
9. Using the npn transistor model of below figure, consider the case of a transistor for which the base is connected to ground, the collector is connected to a 10-V dc source through a 2-Kohm resistor, and a 3-mA current source is connected to the emitter with the Polarity so that current is drawn out of the emitter terminal. If β = 100 and Is =10^{-15}A. Find the voltages at the emitter and the collector and calculate the base current.



10. A transistor characterized by the Ebers – Moll model which is operated with both emitter and collector grounded and a base current of 1mA. If the collector junction is 10 times larger than the emitter junction and α_F =1, find i_C and i_E.
11. A pnp transistor has v_{EB} = 0.8V at a collector current of 1A.What do you expect v_{EB} to become i_C=10mA? At i_C=5A?
12. A pnp transistor modeled with the circuit in below figure is connected with its base at ground, collector at -1.5v, and a 10mA current injected into its emitter. If it is said to have β =10, what are its base and collector currents? In which direction do they flow? If Is =10^{-16}A, what voltage results at the emitter? What does the collector current become if a transistor with β=1000 is substituted?



13. A pnp power transistor operates with an emitter to collector voltage of 5V, an emitter of 10Aand V_{EB}=0.85 V. For β=15, what base current is required? What is I_s for this transistor? Compare the emitter base junction area of this transistor with that of a small signal transistor that conducts i_c=1mA with V_{EB}=0.70v.How much larger is it?
14. A BJT for which BV_{CBO} is 30v is connected as shown in figure. What voltages would you measure on the collector, base, emitter?



15. For a particular npn transistor operating at a V_{BE} of 670 mV and I_c=3mA, the i_C –V_{cE} characteristic has a slope of $3*10^{-5}$mho.To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 30mA what would the output resistance become?

C. Questions testing the analyzing/evaluating ability of students

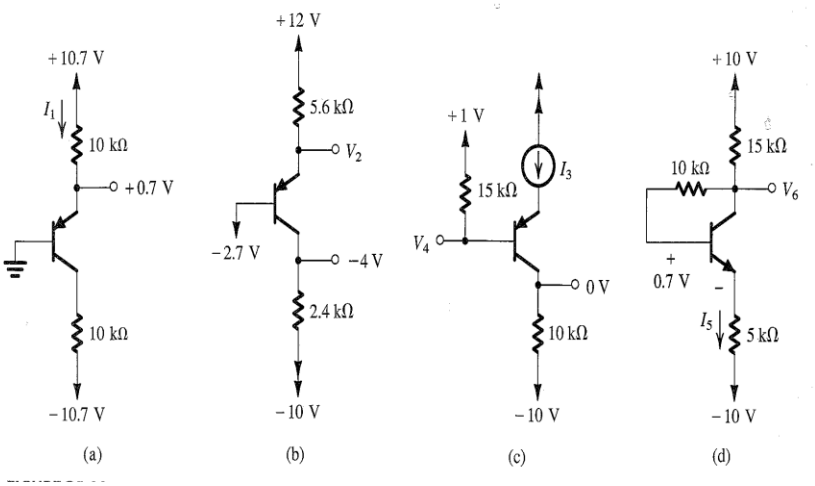
1. The terminal voltages of various npn transistors are measured during operation in their respective circuits with the following results:

case	E	B	C	Mode
1	0	0.7	0.7	
2	0	0.8	0.1	
3	-0.7	0	0.7	
4	-0.7	0	-0.6	
5	0.7	0.7	0	
6	-2.7	-2.0	0	
7	0	0	5.0	
8	-0.10	5.0	5.0	

In this table, where the entries are in volts, indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

2. For the circuits in Fig. shown below, assume that the transistor have very large β. Some measurements have been made on these circuits, with the results indicated in the figure. Find the values of the other labeled voltages and currents.

16.



C. GATE Questions

1. In MOSFET operating in saturation region, the channel length modulation effect causes

   a) an increase in gate source capacitance (GATE 2013) [ ]

   b) decrease in transconductance

   c) decrease in unity gain bandwidth product

   d) decrease in output resistance

2. If the fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to (GATE 2014) [ ]

   a) decrease in threshold voltage b) channel length modulation

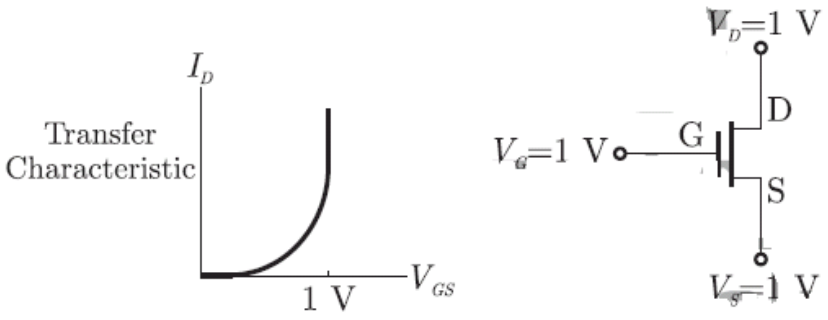
   c) increase in substrate leakage current d) increase in accumulation capacitance

3. The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain-source voltage of 5 V. When the drain-source voltage was increased to 6 V while keeping gate-source voltage same, the drain current increased to 1.02 mA. Assume that drain to source saturation voltages is much smaller than the applied drain-source voltage. Find the channel length modulation parameter λ (in V^{-1}).

   (GATE 2015)

4. The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of the MOSFET is 1 V. If the drain current (I_D) is 1 mA for V_{GS} = 2 V, then for V_{GS} = 3 V, find the value of drain current. (GATE 2004)

5. For an n-channel MOSFET and its transfer curve shown in the figure, the threshold voltage is _____ [ ] (GATE 2005)



a) 1 V and the device is in active region

b) −1 V and the device is in saturation region

c) 1 V and the device is in saturation region

d) −1 V and the device is an active region

6. An n-channel depletion MOSFET has following two points on its I_D–V_{GS} curve:

(i) V_{GS} = 0 at I_D = 12 mA and (ii) V_{GS} =−6 Volts at I_D = 0 mA

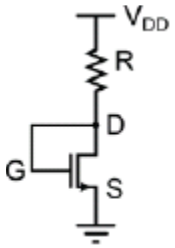
Which Q point will give the highest transconductance gain for small signals?(GATE 2006)

7. When the gate-to-source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, find the drain current for an applied V_{GS} of 1400 mV. (GATE 2003)

8. The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of the MOSFET is 1 V. If the drain current (I_D) is 1 mA for V_{GS} = 2 V, then for V_{GS} = 3 V, find I_D. (GATE 2004)

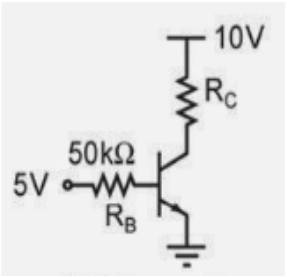
9. For the n-channel MOS transistor shown in the figure, the threshold voltage V_{Th} is 0.8V. Neglect channel length modulation effects. When the drain voltage V_D = 1.6V, the drain

current was found to be 0.5mA. If V_D is adjusted to be 2V by changing the values of R and V_{DD}, find the new value of I_D (in mA). (GATE 2014)



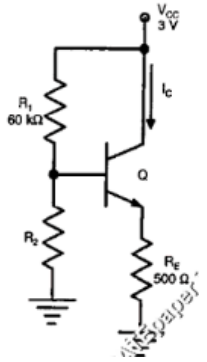
10.. In the circuit shown, the silicon BJT has β = 50. Assume V_{BE} = 0.7v and V_{CEsat} =0.2v. Which one of the following statements is correct? (GATE 2014) [ ]

a) For Rc = 1KΩ, the BJT operates in saturation region
b) For Rc = 3KΩ, the BJT operates in saturation region
c) For Rc = 20KΩ, the BJT operates in cutoff region
d) For Rc = 20KΩ, the BJT operates in linear region



11. In the circuit shown below, the silicon NPN transistor Q has a very high value of β. The required value of R2 in KΩ to produce Ic = 1mA is (GATE 2013)
[ ]

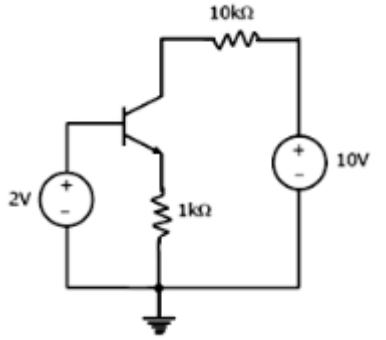
a) 20 b) 30 c) 40 d) 50



12.For a BJT, the common base current gain α = 0.98 and the collector base junction reverse bias saturation current, Ico = 0.6μA. This BJT is connected in the common emitter mode and operated in the active region with a base current I_B of 20 μA. The collector current Ic for this mode of operation is (GATE 2011) [ ]

a) 0.98 mA b) 0.99 mA c) 1.0 mA d) 1.01 mA

13. For the BJT circuit shown, assume that the β of the transistor is very large and V_{BE} is 0.7V. The mode of operation of the BJT is (GATE 2007) [ ]

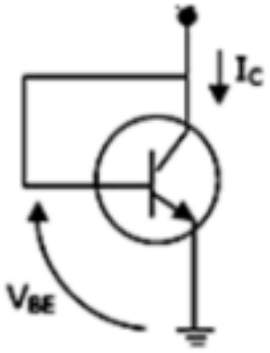


a) cut off
b) Saturation
c) Normal active
d) Inverse active

14. For an NPN transistor connected as shown in figure , V_{BE} is 0.7v. Given that reverse saturation current of the junction at room temperature 300 ^{o}K is 10^{-13} amp, the emitter current is

(GATE 2005) [ ]

a) 30 mA
b) 39 mA
c) 49 mA
d) 20 mA



15.The circuit using a BJT with β = 50 and V_{BE} = 0.7 V is shown in figure. The base current I_B and the collector voltage V_C are respectively _____

[ ]

a) 43 µA and 11.4 volts
b) 40 µA and 16 volts
c) 45 µA and 11 volts
d) 50 µA and 10 volts